FIELD ENGINEERING

TECHNICAL MANUAL

SPD™ 10/20

STORED PROGRAM DISPLAY

INCOTERM Corporation

FS 002

SPD™

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FOREWORD

This manual provides the installation, theory of operation and maintenance procedures for the SPD™ -10/20 stored Program Display Terminal. Field repair is accomplished by on-site replacement of a faulty module. Module repair is performed off-site by a technical staff with appropriate test equipment. An understanding of the theory provided in this manual and a familiarization with the logic diagrams provided in support document FS 003 will provide the required background for technical proficiency in both areas of SPD 10/20 maintenance.

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SPD 10/20 Stored Program Display Terminal

CHAPTER I

INTRODUCTION

1.1 SCOPE

The purpose of this manual is to provide Field Engineers with preliminary data concerning the SPD 10/20 Stored Program Display Terminal. Two levels of information are required within the Field Service organization. First, the Field Repair philosophy dictates repair by replacement of assemblies and subassemblies; and, secondly, Depot repair requires replacement of components in assemblies and subassemblies returned from the field. This manual is organized to fulfill both levels of maintenance.

1.2 GENERAL SPECIFICATIONS

The SPD 10/20 is a CRT display containing a stored-program computer. The built in computer allows the terminal to be programmed and optimized for any specific application. It also allows the terminal to operate in any network, with or without a central computer. Table 1-1 contains the operating specifications for the SPD 10/20 Display Terminal. Table 1-2 provides both physical and electrical data for the Display Terminal and associated products.

1.3 CONFIGURATION

The SPD 10/20 is designed for maximum production standardization such that the product baseline is manufactured and stocked as an off-the-shelf

item. The terminal computing circuitry, Display CRT, input output wiring, and housing are included in the baseline configuration. When a customer's order is placed, any required additional hardware is easily included. Configuration deviations are caused by each customer's definition of the type of data environment the Terminal will be exposed to. At this point, modular I/O interface circuitry is added with little or no change necessary to the manufactured terminal.

1.3.1 Minimum Configurations

Minimum unit configuration relative to the SPD 10/20 product line is comprised of three terminal utilizations, illustrated in Figure 1-1. First, the basic terminal contains the terminal processor (computer), display, keyboard and half duplex communications interface. The second adds a remote display and keyboard manufactured as an auxiliary unit to the basic terminal. The auxiliary is identical in appearance to the basic unit, but does not have a computer or I/O circuitry. The basic terminal, in this case, becomes a master; the auxiliary is a slave that shares the basic terminal computer. The third is a further extension of the second, which results in two additional input and display stations operating as slaves to the master terminal.

1.3.2 Units Available for Expanded Configurations

As an enhancement to the versatility of the SPD 10/20 Display Terminal, INCOTERM has developed a complete family of SPD products. The following paragraphs briefly describe each product. Figure 1-2 illustrates the present SPD product line.

SPD™-L Program Loader

The SPD-L Program Loader is used to load data into the TPU from punched paper tape. The loader, a portable device, contains its own control electronics and does not require an I/O interface controller. Data is entered into the TPU by bootstrapping the tape data to the I/O data bus, which is directly accessed at connector 9 on the TPU connector panel. This mode of operation is initiated at the loader. It is possible to load from tape via TPU command.

Table 1-1. SPD 10/20 Terminal Processing Unit (TPU) Specifications

Type:	Parallel binary, byte oriented
Addressing:	Single address with indirect addressing
Data Word Length:	8-bit byte, 12-bit special word
Memory Word Length:	16 bits, 2 bytes
Arithmetic Code:	Two's complement
Internal Memory:	Magnetic core with 2048 16-bit words
Memory Cycle:	1.6 microseconds
Machine Speed:	Add: 3.2 microseconds Subtract: 3.2 microseconds
Standard I/O Lines:	8-bit input bus 8-bit output bus 10-bit control bus 8 interrupt lines

SPD™ -M Terminal Multiplexer Unit

The SPD-M provides the capability of interfacing a maximum of 16 terminals to a single modem. When in use, the Multiplexer monitors the communications line and provides ordered transmissions. The Multiplexer can also be cascaded to provide additional terminals with data.

SPD™ -P Printer

The SPD-P is a hard copy output device which prints out messages sent to it by SPD 10/20 Terminals. The Printer contains its own multiplexer and can interface with up to 16 SPD 10/20 Terminals. The hard copy form is edge sprocketed measuring up to 14-7/8 inches in width and 11 inches in length. The forms can provide multiple copies. Data input to the Printer conforms to the American Standard Code for Information Interchange (ASCII).

1.4 REFERENCE DOCUMENTS

SPD 10/20 programming instructions are found in the Programmer's Reference Manual. Operating functions for specific programs are found in

Table 1-2. SPD Product Physical and Electrical Data

Unit Type	Size in Inches (HxWxD)	Weight in Lbs.	Maximum Cable Length in Feet	Power in Watts	Voltage & Frequency
SPD 10/20	18x18.5x19	48	50 - Modem 300 - Multiplexer 1000 - Multiplexer (OPTIONAL)	180	117V ±10%, 60± 1 Hz
KEYBOARD	3.2x19x8.1	7	10 - SPD 10/20	POWERED FROM SPD 10/20	
PRINTER	12x31x26 (Desk) 36x31x26 (Pedestal)	90	300 - SPD 10/20 1000 - SPD 10/20 (OPTIONAL)	450	110 to 125V, 60 ±0.5 Hz
MULTIPLEXER	9.5x17x14	30	50 - Modem 300 - SPD 10/20 1000 - SPD 10/20 (OPTIONAL)	120	117V ±10%, 60± 1 Hz
PROGRAM LOADER	5x12x7	10	10 - SPD 10/20	POWERED FROM SPD 10/20	
AUXILIARY DISPLAY	18x18-1/2x19	40	10 - SPD 10/20	60	117V ±10%, 60± 1 Hz

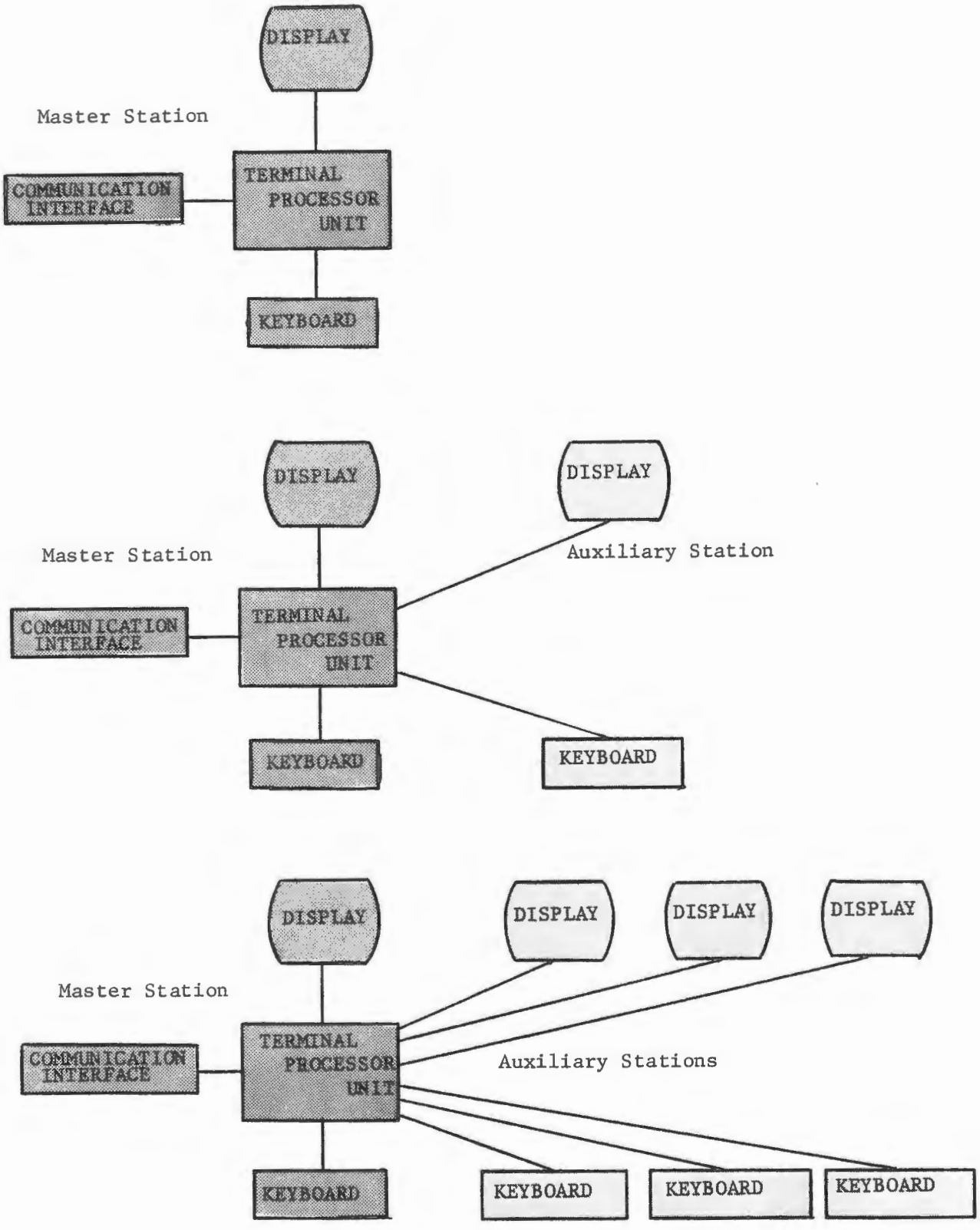


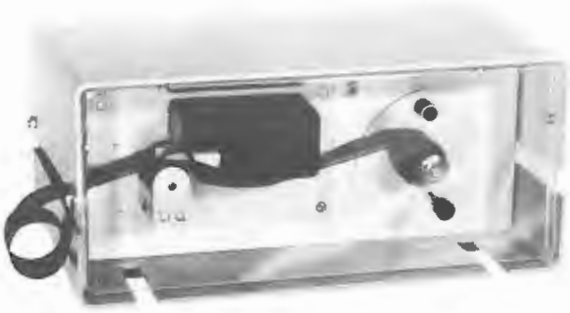
Figure 1-1. Minimum Terminal Configurations

SPD-P Printer

SPD-M Multiplexer

SPD-10/20 Stored Program Display

SPD-T Tape Cassette



SPD-L Program Loader

Figure 1-2. SPD Product Line

the Operator's Brochure. Integrated circuit descriptions are found in Texas Instrument Catalog CC-201R and supplement CC-301. Technical data for the SPD Peripheral line is presented in the INCOTERM Peripheral Products Technical Manual.

CHAPTER II

INSTALLATION

2.1 VISUAL INSPECTION

Prior to unpacking, check the shipping container for signs of damage in shipment such as crushed or torn areas. Packing at the factory consists of placing the Terminal on a plywood base which prevents lateral movement during shipment. The Terminal is then placed in a cardboard container which serves as an inner container. The inner container is restricted from moving within the outer container by edgemounted shock absorbers. See Figure 2-1 for packaging layout.

As illustrated in Figure 2-1, the Keyboard and associated cables are packed in a separate smaller container. Shipping weight of the Terminal is approximately 60 pounds. Shipping weight of the Keyboard and cables is approximately 10 pounds.

In the event that damage in shipment has occurred or the items received are not those listed on the Equipment Summary, promptly contact:

James Mahoney
INCOTERM Corp.
Phone: 617-481-2000

A visual examination of the contents can be made while removing the Terminal from the shipping container. Check for any indication of damage in shipment, such as cracked outer housing, broken CRT, damaged cables,

pins, loose or bent hardware, etc. Remove the plywood base and outer housing from the Terminal to facilitate visual inspection of the bottom and inside of the Terminal.

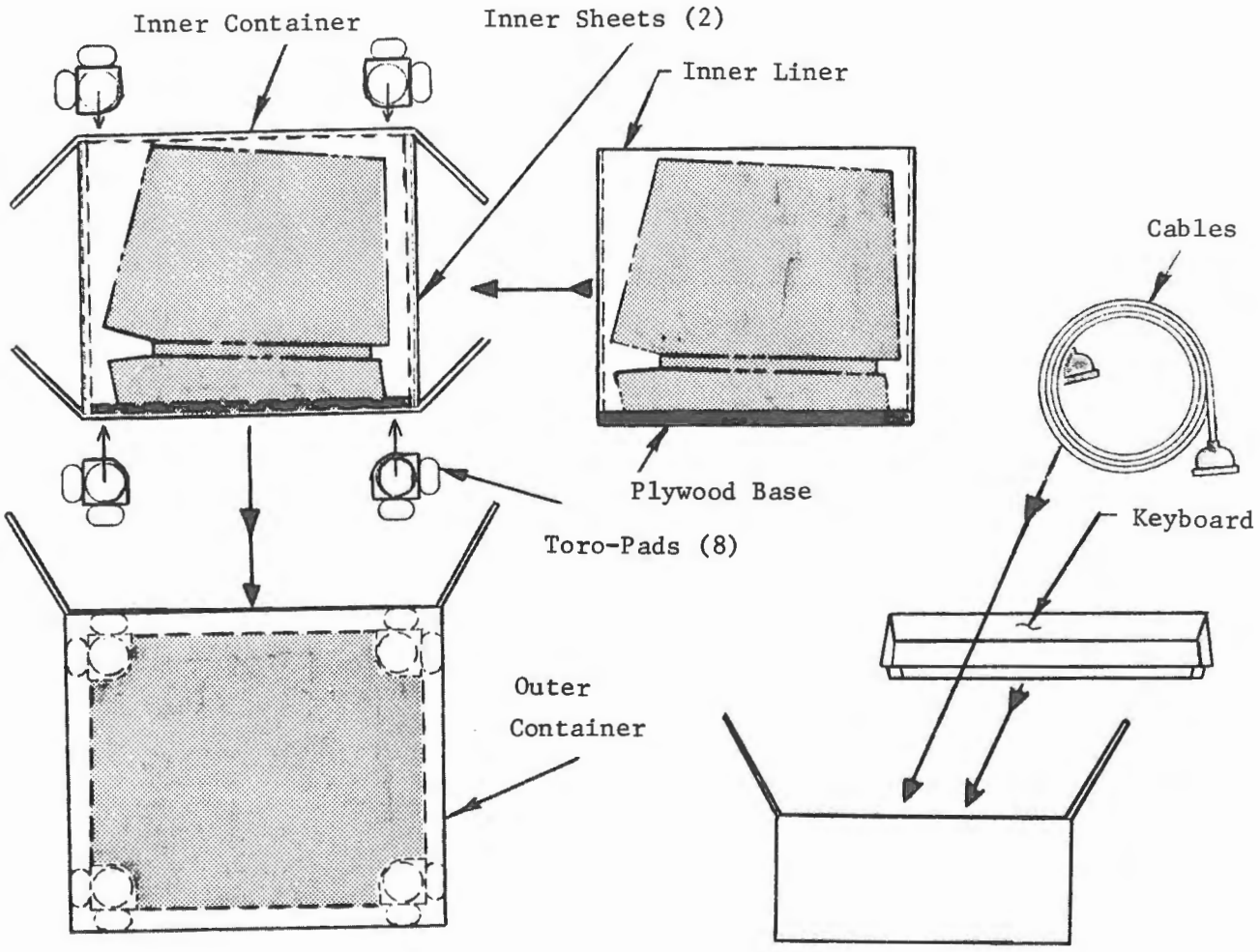


Figure 2-1. Factory Packing

Removal of the outer housing is accomplished as follows. (See figure 2-2.)

(a) Place Monitor protective pad on table and rest Terminal face down on the pad.

(b) Remove plywood base by removing four retaining bolts.

(c) Rotate the two lock-down screws located under the rear edge of the Terminal.

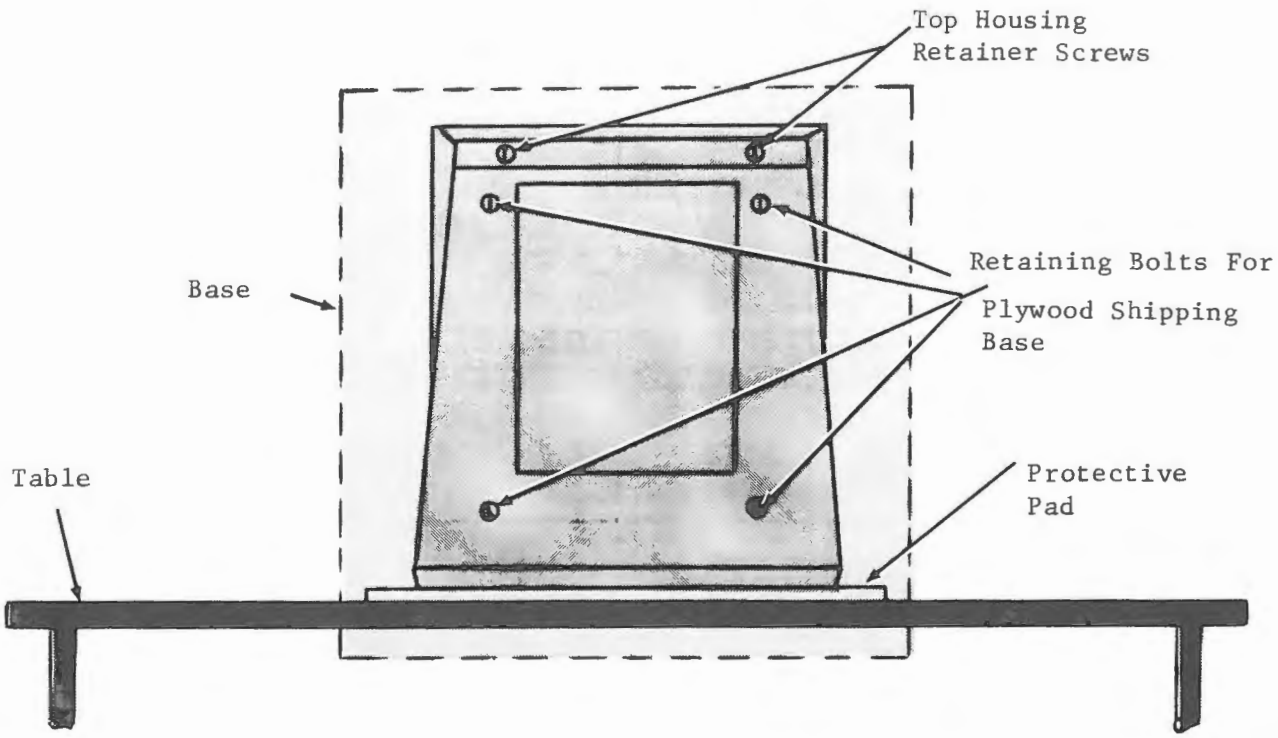


Figure 2-2. Removal of Plywood Base

(d) Return the Terminal to its proper position and lift outer housing up and away from Terminal.

While the top cover is off, check the circuit boards to see if they are properly aligned and plugged in, as vibration in shipment could cause board loosening. See Figure 2-3 for circuit board identification and location. Check the connectors and fuses that are accessible from the bottom of the Terminal. See Figure 2-4 for identification and location. Replace top cover by reversing the removal procedure. Figure 2-5 and 2-6 provide actual views relating to construction and location of the TPU and associated components.

2.2 CONFIGURATION CHART

Table 2-1, along with the visual inspection and shipping memo (Figure 2-7), provide a check list to verify that for the given product, model and serial number, the required boards have been supplied. This table will be expanded as future products, models and options are developed.

Slot ID No.	Board Name	Slot ID No.	Board Name
1.	Keyboard Controller	9.	SPARE (no connector)
2.	Half Duplex Communications Controller	10.	Memory Electronics
3.	*	11.	Memory Stack
4.	*	12.	CPU Data Flow
5.	*	13.	CPU Control
6.	*	14.	Refresh Memory and Timing Unit
7.	*	A	Power Supply 'A' Board
8.	*	B	Power Supply 'B' Board

* Space for Additional Controller Options or Features

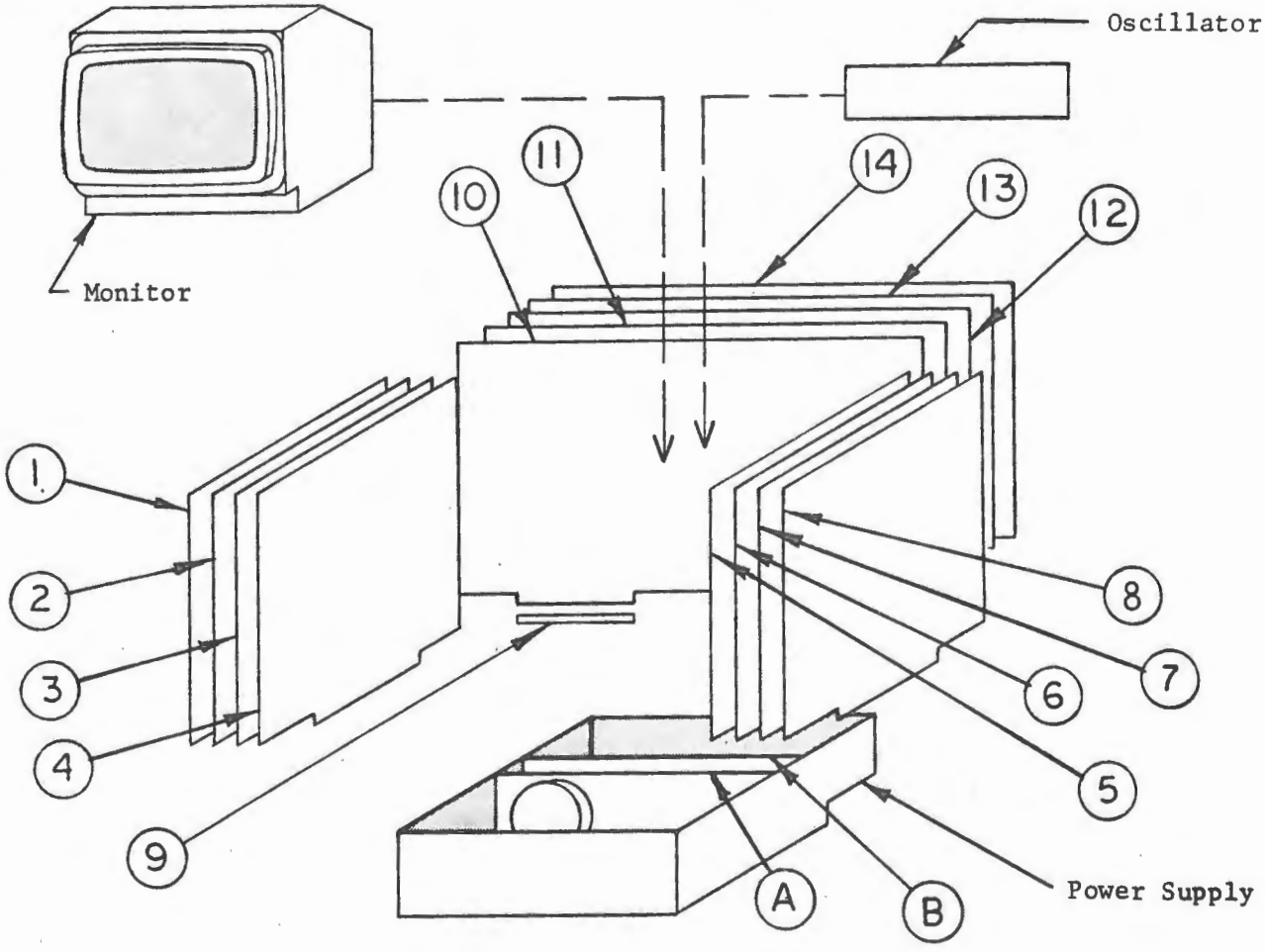
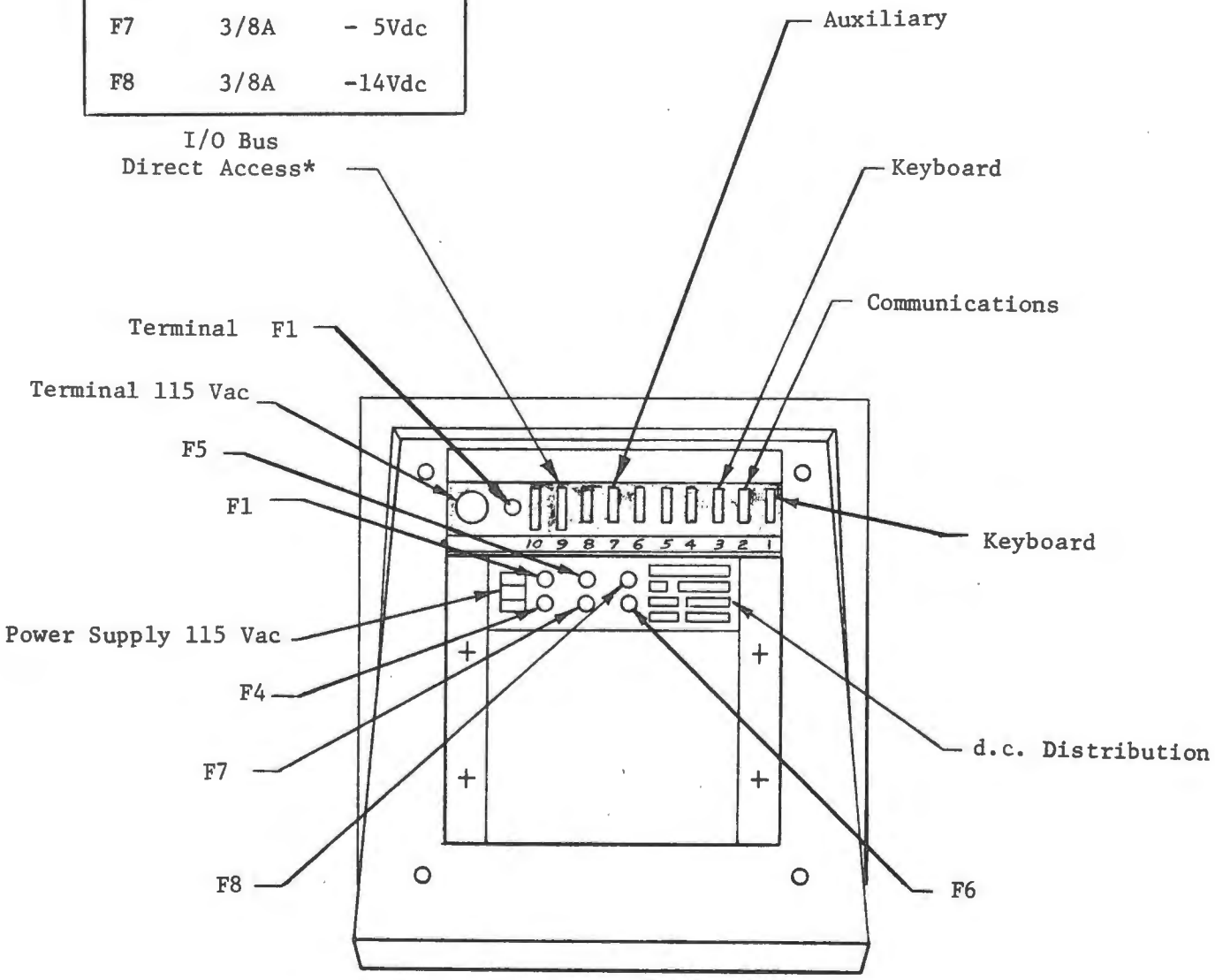


Figure 2-3. Circuit Board Identification and Location

POWER SUPPLY			TERMINAL		
FUSE	VALUE	VOLTAGE	FUSE	VALUE	VOLTAGE
F1	2.5A	117Vac	F1	3A	117Vac
F4	1.5A	+25Vdc			
F5	3A	+14Vdc			
F6	10A	+ 5Vdc			
F7	3/8A	- 5Vdc			
F8	3/8A	-14Vdc			



* Will commonly be used for Program Loading.

Figure 2-4. Bottom View of Terminal Showing Connector Panel and Fuses

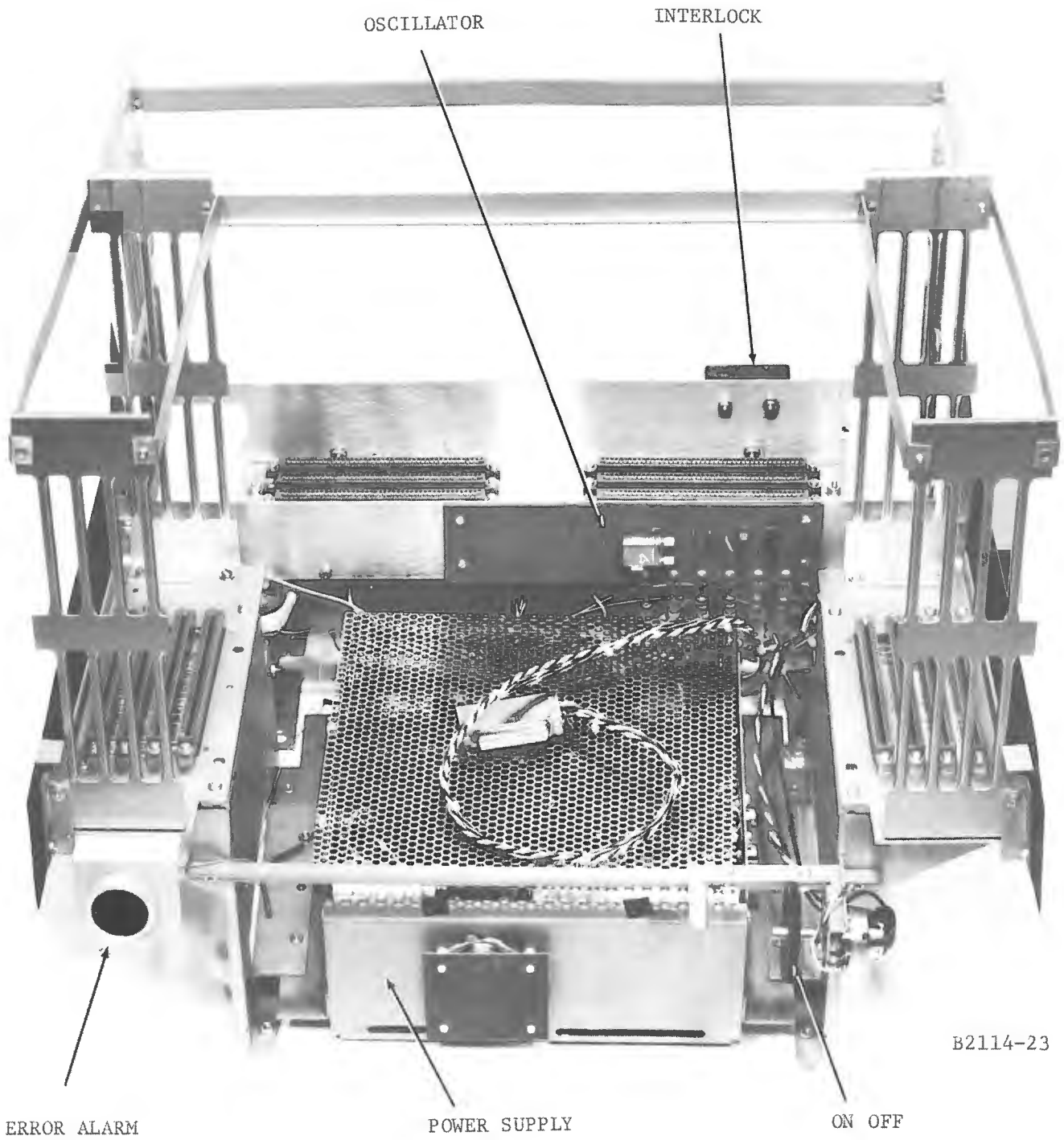


Figure 2-5. TPU Wired Chassis with Power Supply

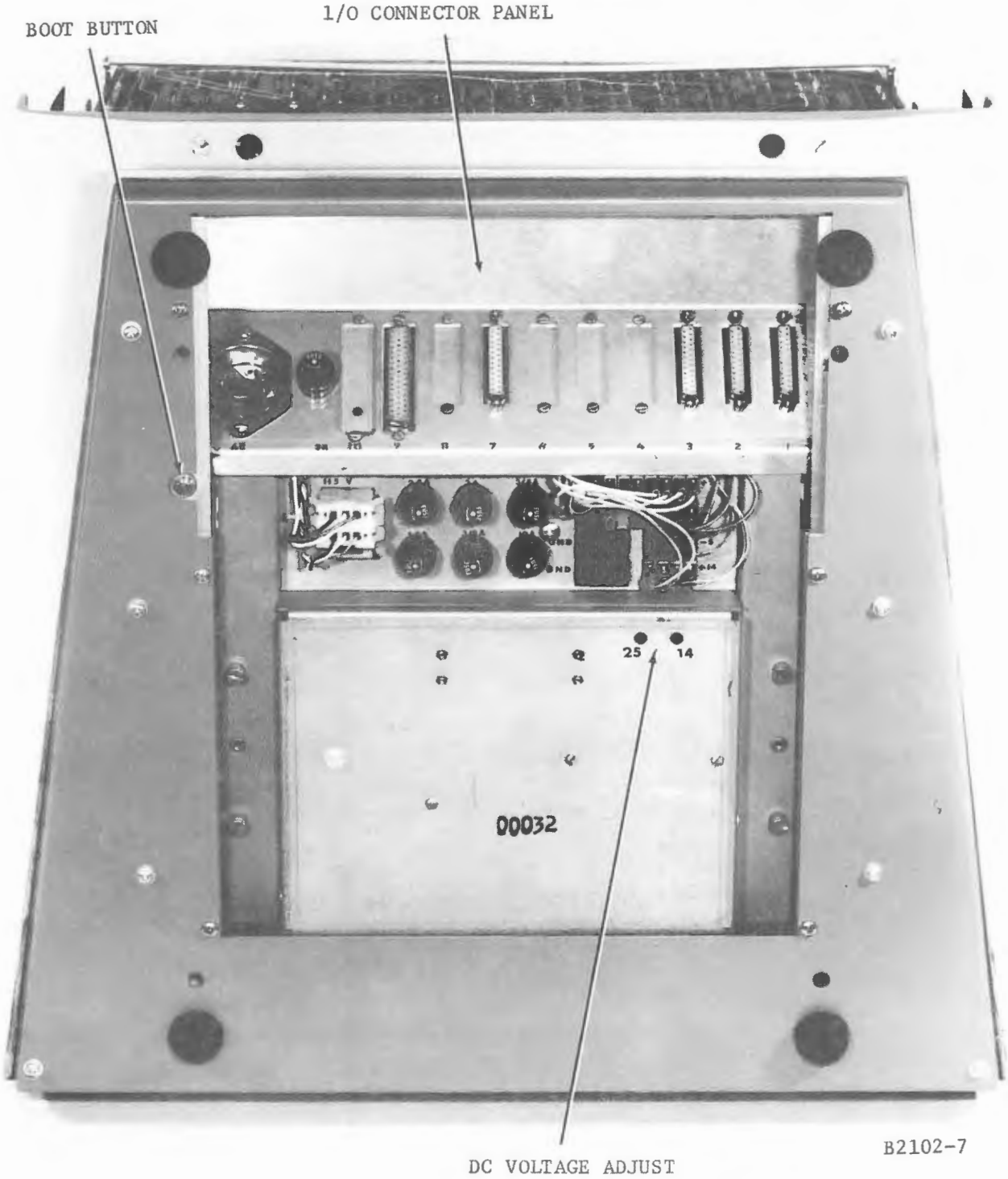


Figure 2-6. Bottom View Actual Photo

Table 2-1. Configuration Chart

Board Slot	Circuit Board Allocation per Product and Model Number				
	005/00010	006/00011	005/00012	006/00013	005/00014
1.	Keyboard 001-03-03	Keyboard 001-03-03	Keyboard 001-03-03	Keyboard 001-03-03	Keyboard 001-03-03
2.	Sync 001-08-03	Sync 001-08-03			Sync 001-08-03
3.	Keyboard 001-03-03	Keyboard 001-03-03			
4.					
5.					
6.					
7.	Split Screen 001-15-03	Split Screen 001-15-03	Jumper	Jumper	Jumper
8.					
9.	← NO CONNECTION →				
10.	Memory Elec. 001-06-03	Memory Elec. 006-06-03	Memory Elec. 001-06-03	Memory Elec. 006-06-03	Memory Elec. 001-06-03
11.	Memory Stack 2K	Memory Stack 2K	Memory Stack 2K	Memory Stack 2K	Memory Stack 2K
12.	TPU Data Flow 001-02-03	TPU Data Flow 006-02-03	TPU Data Flow 001-02-03	TPU Data Flow 006-02-03	TPU Data Flow 001-02-03

Table 2-1. Configuration Chart (Cont)

Board Slot	Circuit Board Allocation per Product and Model Number				
	005/00010	006/00011	005/00012	006/00013	005/00014
13.	TPU Control 005-07-03	TPU Control 005-07-03	TPU Control 005-07-03	TPU Control 005-07-03	TPU Control 005-07-03
14.	Refresh Module and Timing Unit 005-14-03	Refresh Module and Timing Unit 005-14-03	Refresh Module and Timing Unit 005-14-03	Refresh Module and Timing Unit 005-14-03	Refresh Module and Timing Unit 005-14-03 (Custom)
With AUX	X	X			
Without AUX			X	X	X

NOTE

Board etch number is listed in Table 2-1 because there is a difference between Product 005 and 006 art work. The Table makes the different boards clear. Also be aware that the number etched on a given board relates to the artwork and is not a circuit board part number. The part number is provided on the Equipment Summary.

Figure 2-7 is an example of the Shipping Memo which is packed with each system. As stated previously, this data is available at installation time. The data identifies the particular Terminal and should be retained for future reference.

2.3 SITE PREPARATION

Site preparation is not a critical factor with the SPD 10/20 Terminal. Verify that the site contains a 115 VAC, 60 Hz, 3 wire (hot, common and ground) connector and a cable for connecting the Terminal to the selected communications device, such as a modem. This cable is supplied by INCOTERM at the customer's request.

2.4 INSTALLATION

On-site installation of the SPD 10/20 Terminal requires connecting the cables to the rear of the Terminal, and to external equipment. As indicated in Table 2-1, these instructions are directed toward initial Product Installation.

2.4.1 Cabling of Product 005, Model 00010

The SPD 10/20 Terminal, Model 00010 configuration consists of a Master Terminal and an Auxiliary Terminal. Each Terminal has a Keyboard Controller, Video Display and Keyboard input unit; however, both Terminals share a single Processor that is contained in the Master unit. Figure 2-8 is a cabling diagram for the Model 00010.

The following instructions define the cable connections required to install an SPD 10/20 Terminal in the Product 005, Model 00010 configuration. Throughout the entire cabling procedure observe proper cable dressing for professional final appearance. Secure each cable with connector hood securing screws. Proceed as follows to install the cabling.

(a) Position the INCOTERM equipment on the desk or table designated by the customer.

(b) Position a Keyboard in front of the Master Display and connect the Keyboard cable (male end) to the Display rear connector number 1. Route the female end under the

INCOTERM CORPORATION

SHIPPING MEMO NO. 1111A

HAYES MEMORIAL DRIVE, MARLBOROUGH, MASS. 01752 617-481-2000 TELEX 94-8402

SHIPPING MEMO

SHIP TO
FRIENDSHIP AIRPORT
Baltimore, Maryland
Hold for Pick-up by Jack Colburn
of Incoterm Corporation

SAMPLE

PURCHASE ORDER NO.	SALES ORDER NO.	DATED	DEFECTED MAT'L. REPORT NO.

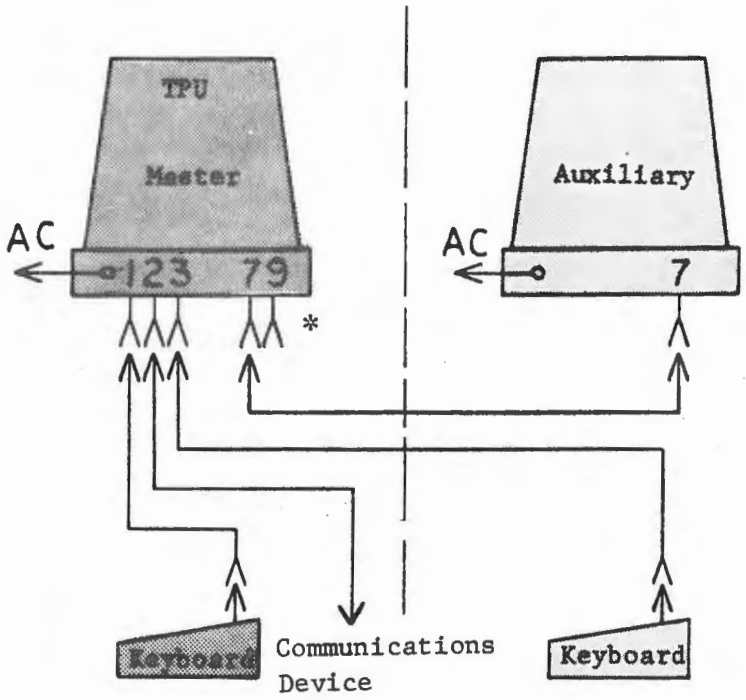
DATE OF SHIPPER	SHIP NOT LATER THAN	TRANSPORTATION CHARGES	SHIPPED VIA	WEIGHT	DATE SHIPPED	CHECKED BY
			Air Freight		12/18/70	

ITEM	QUANTITY ORDERED	QUANTITY SHIPPED	DESCRIPTION	UNIT COST	TOTAL
1.		2	SPD 10/20 Data Terminals Serial #'s 135 & 124		
2.		2	Keyboards Model #2-702 Serial #'s 173 & 108		
3.		2	Keyboard Cables		
4.		2	Power Cords		
5.		1	Paper Tape Reader. Model #3-701 Serial #117		
6.		1	Paper Tape Cable		
			NOTE: Supplied by Marketing for DEMO		

TOTAL MATERIAL CHARGES	
TRANSPORTATION CHARGES	
INSPECTION CHARGES	
PACKAGING CHARGES	
OTHER MISC. CHARGES	
TOTAL DEBIT	

Figure 2-7. Sample Shipping Memo

THIS IS NOT A PURCHASE ORDER



*Connector Number 9 is Wired Directly to the I/O Bus and is Generally Used for Program Loading.

Figure 2-8. Cabling Diagram for Model 00010

Master Display then to the Keyboard. Also on the Keyboard end, locate the white 9-pin nylon plug and connect it to the nylon connector (this provides power to the Master Keyboard lamps).

(c) Position a Keyboard in front of the Auxiliary Display and connect the Keyboard cable (male end) to rear connector number 3 of the Master Display. Route the female end under the Auxiliary Display, then connect it to the Keyboard. Also on the Keyboard end, locate the white 9-pin nylon plug and connect it to the nylon connector (this provides power to the Auxiliary Keyboard lamps).

(d) Connect Auxiliary Display connector number 7 to Master Display connector number 7, utilizing the double female cable provided.

(e) Connector number 2 is dedicated to communications I/O operations. Connect the cable to the specified communications device.

(f) Connector number 9 is wired to accept Program Loader inputs. If the Loader is used, connect 50-pin female connector from the Loader unit to connector number 9.

(g) Tighten any loose cabling hardware and check interlock switch for proper engagement with actuating arm.

(h) Check customer ac line for proper voltage and ground.

(i) Attach twist lock ac line cords to both displays.

(j) Plug line cords into outlet.

2.4.2 Cabling of Product 006, Model 00011

As derived from Table 2-1, the circuit board complement in this model is identical to the 00010 model. The prime difference is the connector pin compatibility on the Memory Electronics and Data Flow Boards, which are not interchangeable between models. This difference is of no importance during installation. Refer to Figure 2-8 and follow the cabling instructions in paragraph 2. 5. 1.

2.4.3 Cabling of Product 005, Model 00014

Unlike Models 00010 and 00012, the Model 00014 is not configured to operate with the auxiliary capability. Installation cabling is illustrated in Figure 2-9.

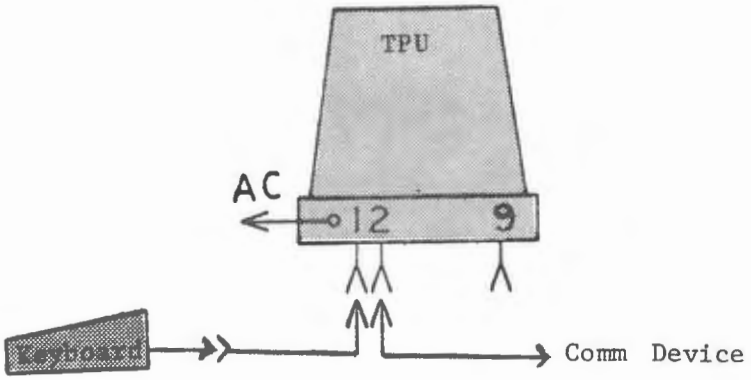


Figure 2-9. Cabling Diagram for Model 00014

Proceed as follows to install the cabling.

(a) Position the INCOTERM equipment on the desk or table designated by the customer.

(b) Position the Keyboard in front of the Terminal and connect the Keyboard cable male end to the Display rear connector number 1. Route the female end under the Display then to the Keyboard. Also on the Keyboard end, locate the white 9-pin nylon plug and connect it to the nylon connector (this provides power to the Keyboard lamps).

(c) Connector number 2 is dedicated to communications I/O operations. Connect the cable to specified communications device.

(d) Connector number 9 is wired to accept Program Loader inputs. If the Loader is used, connect 50-pin female connector from the Loader unit to connector number 9.

(e) Tighten any loose cabling hardware and check interlock switch for proper engagement with actuating arm.

(f) Check customer ac line for proper voltage and ground.

(g) Attach twist-lock ac line cord to Display.

(h) Plug line cord into outlet.

CHAPTER III

OPERATION

3.1 GENERAL INFORMATION

A Power On switch and a keyboard are the only controls required to operate the SPD 10/20 Display Terminal. The Power On switch is located on the under side of the display at the front right. It is a rotary switch that is also used to adjust the brightness of the display screen.

The keyboard contains the keys, controls and indicators necessary to operate and monitor the display. It is connected to the display with a ten-foot cable that allows convenience in positioning the keyboard. The operator uses the keyboard to input data to the Terminal Processor Unit via an I/O interface called a Keyboard Controller. The formatting of input data and operation of the special function keys are predetermined by the stored software program.

3.2 KEYBOARD

3.2.1 Introduction

The stored software program determines the functions that the operator can enable via the keyboard. The programs vary with customer applications so that it is not possible to describe a standard keyboard configuration. The keyboard described is for a specific application but it can be considered typical for this discussion.

3.2.2 Key Functions

All keyboards conform to a single physical layout (see Figure 3-1). The center section consists of four rows of keys and a space bar. The bottom row contains 12 keys and the other three rows contain 13 keys each. Twelve function keys are located on each side of the center section. Unused keys are not engraved.

The center section of the keyboard contains the alphanumeric keys and is arranged essentially the same as a standard electric typewriter keyboard. The alphabet is used in upper case only. The SHIFT key has no effect on these characters. Other keys in this group have both upper and lower case characters. They must be used in conjunction with the SHIFT key to obtain the upper case character. When a key is depressed, the character engraved on its top is displayed on the CRT at the cursor location.

The special keys are described below.

DATA CONTROL KEYS

MSG WAITING	Requests a waiting processor message when MSG WAITING indicator is lit. When this key is depressed, the keyboard is locked until completion of message.
TRANS	Causes the message displayed on the CRT, starting from the START OF ENTRY symbol ▷ and continuing forward to the cursor, to be transmitted to the processor. If there are multiple ▷ symbols displayed, transmission begins at the nearest ▷ to the left of the cursor. If no ▷ symbols are displayed, transmission begins at line 1, character 1 position. Keyboard is locked until message transmission is completed.
RESET	Causes the keyboard to unlock and should be used with discretion to prevent interruption of message transmission and receipt.
PRINT	Causes the message displayed on the CRT, starting from the ▷ symbol and continuing forward to the cursor, to be printed on the locally attached output printer. If there are multiple ▷ symbols displayed, printing begins at the nearest ▷ symbol to the left of the cursor. If no ▷ symbols are displayed, printing begins at the home position. Keyboard is locked until printing is completed.
TAB SET	Inserts a TAB STOP character in the memory position occupied by the cursor. The cursor will automatically move one position to the right, after tab is set.

B2114-18

Figure 3-1. Typical Keyboard Arrangement

EDITING KEYS

Editing keys are used to make changes in the text message prior to transmission. The cursor must be at the character position where the action is to be taken; viz., deleted, inserted or erased.

ERASE END DISPLAY — Erases and enters spaces in all character positions including the cursor position to the end of the display.

ERASE END LINE — Erases and enters spaces in all character positions from and including the cursor position to the end of that line.

IN DISPL DELETE IN LINE — Uppercase (depress SHIFT key) operation of this key causes all characters in the display to the right of the cursor to move left one position. The original character at the cursor position is deleted and a space is inserted into the last character position of the display. This key is pressed once for each character deleted.

Lowercase operation of this key causes the characters in the line to the right of the cursor to shift left one position. The original character at the cursor position is deleted and a space is inserted into the last character position in the cursor line. This key is pressed once for each character to be deleted.

IN DISPL INSERT IN LINE — Uppercase (depress SHIFT key) operation of this key causes all the characters in the display from and including the cursor position to move right one position. A space is inserted in the cursor position and if a character is moved out of the last position of the display, it is discarded.

Lowercase operation of this key causes all the characters in the line from and including the cursor positions to move right one position. A space is inserted in the cursor position and if a character is moved out of the last position of the line it is discarded.

Warning: When a space or character is inserted in the cursor position, causing an overflow in the display, the last character(s) will be discarded.

CHAR ERASE — Causes the character at the cursor position to be deleted, inserting a space in lieu of the character. The cursor will not move.

CURSOR CONTROL KEYS

The cursor symbol ▮ is always present and indicates where the next keyboard or processor generated character will appear. These keys are nondestructive.

→	If the key is pressed momentarily, it causes the cursor to move forward one position. If the key is held down, the function is repeated at a rate of approximately 10 cycles per second. If the cursor is at the last character position in a line, it will step to the first position of the next line. If the cursor is in the 64th position of the line 30 (line 15 if dual display), it will move to position one of the first line.
←	If the key is pressed momentarily, it causes the cursor to move backward one position. If the key is held down, the function is repeated at a rate of approximately 10 cycles per second. If the cursor is at the first character position in a line, it will step to the last character position of the previous line. If the cursor is in the first position of line 1, it will move to the last position of line 30 (line 15 if dual display).
↑	If the key is pressed momentarily, it causes the cursor to move up one line in the same character position. If the key is held depressed, the function is repeated at a rate of approximately 10 cycles per second. If the cursor is in the top line, it will step to the bottom line, maintaining the same character position.
↓	If the key is pressed momentarily, it causes the cursor to move down one line in the same character position. If the key is held depressed, the function is repeated at a rate of approximately 10 cycles per second. If the cursor is in the bottom line, it will step to the top line, maintaining its character position.
CURSOR TO HOME	Causes the cursor to move to the first character position on the display (upper left-hand corner).

SPECIAL KEYS

START OF ENTRY	Depress prior to entering input. Causes the start of entry symbol ▷, to be displayed on the CRT. When the message is completed, all data from the ▷ to the cursor is transmitted.
TAB	This special cursor-positioning key moves the cursor forward until a special character, set by the TAB SET key, is detected. The cursor will stop either one space beyond the tab character or at the end of the display if no tab character is found.
SPACE	Pressing this cursor positioning bar places a space in the current cursor position and moves the cursor one character position to the right. If the cursor is in the last position in a line, it moves to the first character position in the next line.
RETURN	Occupies the position normally occupied by the carriage return key on the standard electric typewriter keyboard. Pressing this key causes the cursor to move to the first character position in the next line.

SHIFT LOCK — This key places the keyboard in the uppercase mode. Depression of this key causes the SHIFT LOCK indicator light to turn on. A subsequent depression of the SHIFT LOCK key returns the keyboard to the normal mode and turns off the SHIFT LOCK indicator light.

Also used in conjunction with DELETE and INSERT IN DISPLAY (see Editing Keys).

3.2.3 Indicator Functions

Eight indicator lights are located on the keyboard. They are arranged in a row in the top center position. The indicators are program controlled and are not actuated by the keyboard electronics.

STATUS INDICATOR LIGHTS

MSG WAITING — When the processor has an unsolicited message for display, this light goes on. The indicator remains lit until the MSG WAITING key is depressed to request the message.

WAIT — This indicator light comes on while a message is being transmitted to or received from the processor. In addition, the keyboard remains locked for the entire transmission time. The keyboard is locked whenever the TRANSMIT or PRINT key is depressed and remains locked until a valid text message or print complete signal is received. The processor can effect a keyboard lock by inserting a lock code in a message.

MSG INCOMPL — Lights while text is being received and is automatically turned off when communications error checks are satisfied.

SHIFT LOCK — This indicator lights when the SHIFT LOCK key is depressed and goes off when the SHIFT LOCK key is depressed a second time.

3.3 INITIAL TURN ON AND CHECK OUT

3.3.1 Initial Turn On Procedures and Indications

After installation, activate the SPD 10/20 Terminal by turning on the rotary power switch. The CRT should illuminate approximately 30 seconds after the switch is turned on. The switch can be rotated to control the screen brightness. Screen illumination (raster) indicates that ac power is applied to the Terminal. Proper CRT operation is verified by horizontal and vertical synchronization of the raster.

Assuming that the Terminal contains a stored program, type a few characters on the keyboard. The characters and the cursor should be displayed on the CRT which confirms that the power supply is operating and the Terminal electronics appear normal. Exercise each alphanumeric key by depressing it twice in succession. Observe that the displayed data is in the form QQWWEE, etc. Erase the screen and type a few lines of text. Exercise the editing keys and other special function keys and observe the screen for proper operation. Exercising the keyboard in this way indicates normal operation of some of the Terminal circuitry; particularly, that contained on the Keyboard Controller board. If the installation contains an Auxiliary Terminal, exercising both keyboards checks out the Split Screen Controller as well.

The Communications Controller board is checked by connecting the Terminal to a communications device and performing a dynamic test. Confirm that the communications device and its associated cable are trouble-free prior to testing.

3.3.2 Programmed Operation

If the initial turn-on indications and responses are satisfactory, final checkout is performed by operating the Terminal under control of the customer's software program.

The program can be loaded with the INCOTERM SPD-L Program Loader using the validated tape supplied with the Terminal. Refer to the SPD-L Program Loader Section in the Peripheral Manual for details of operation.

If problems are encountered during programmed operation or initial turn-on, refer to Chapter 6, Maintenance, and Chapter 5, Theory of Operation.

CHAPTER IV

SYSTEM DESCRIPTION

4.1 INTRODUCTION

The SPD 10/20 is a complete unit that contains all the hardware necessary to perform as a remote alphanumeric and/or point-plot graphic display. It interfaces with all common communications equipment through standard modems. It also interfaces with the INCOTERM peripheral devices: SPD-L Program Loader, SPD-P Printer, SPD-M Multiplexer and the SPD-T Tape Cassette. These devices are briefly described in Chapter I. Detailed information can be obtained from the Peripheral Technical Manual associated with each device. System configuration varies with each application; however, a brief discussion of the three minimum configurations (single, dual and quad) is found in Chapter I.

4.2 SYSTEM FUNCTIONAL DESCRIPTION

4.2.1 General Information

The SPD 10/20 Terminal consists of the Terminal Processing Unit (TPU), Interface Controllers, CRT Display Unit and Keyboard Unit. The keyboard is considered as part of the Terminal. Figure 4-1 is a simplified system block diagram.

The Terminal Processing Unit is physically constructed of five printed circuit boards which are identified as memory electronics, memory stack, data flow, control, and refresh module and timing. In Figure 4-1, both

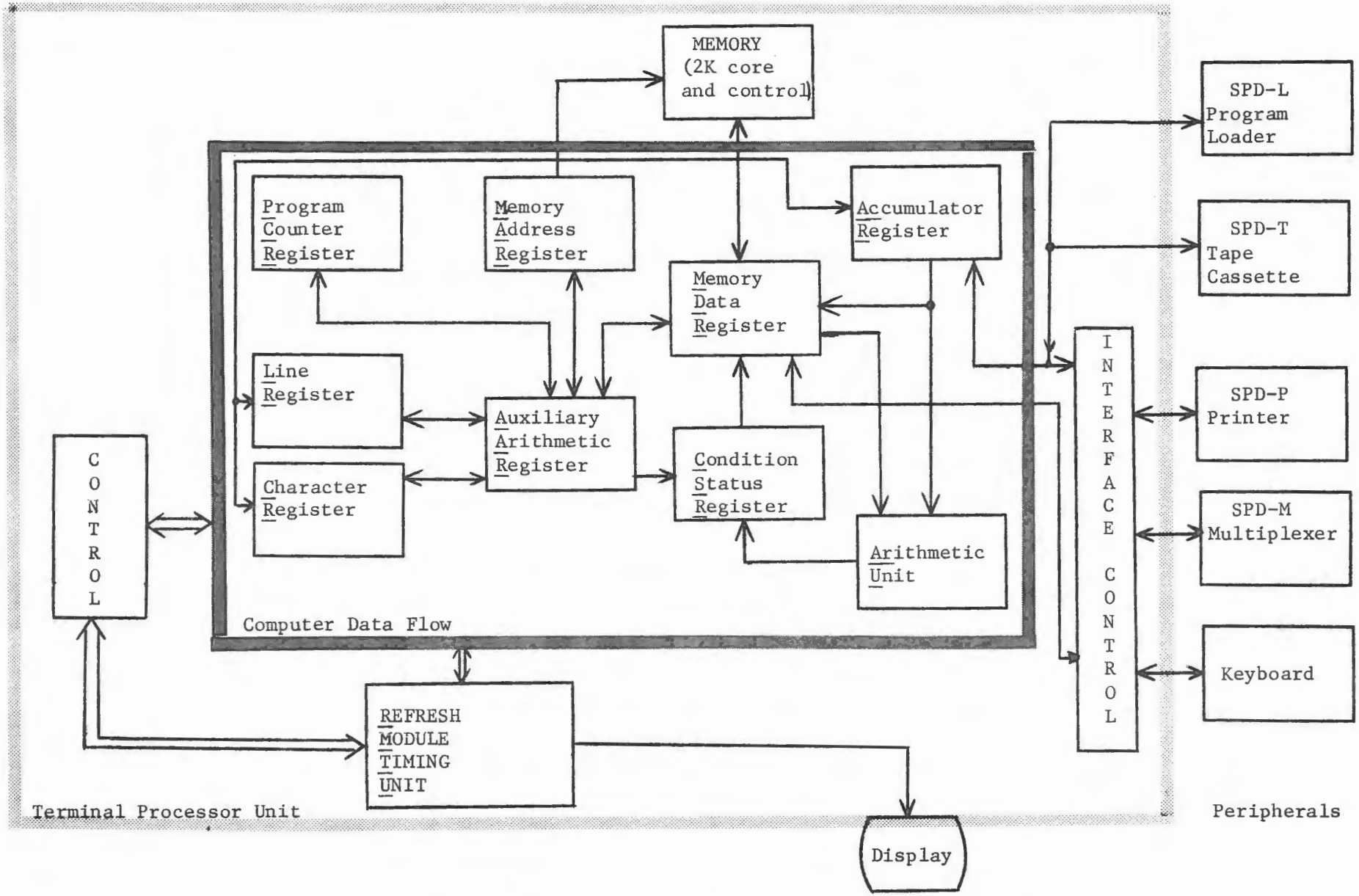


Figure 4-1. SPD 10/20 Stored Program Display System

memory boards have been combined functionally; the Data Flow has been reduced to show the register detail in a system concept. The functional units that are contained on these boards have been identified to show the basic data flow and to introduce the reader to the terminology used in Chapter V, Theory of Operation. The illustration shows a Keyboard, SPD-P Printer, SPD-M multiplexer, SPD-L Program Loader and SPD-T Tape Cassette connected to the Terminal. Each device except the SPD-L and SPD-T require a plug-in Controller to interface with the Terminal. Figure 4-2 shows the printed circuit board arrangement and identification.

4.2.2 Terminal Processing Unit

1. Computer Data Flow (See Figure 4-1)

Memory: The SPD 10/20 utilizes a ferrite core coincident-current memory organized in a 3D-4 wire configuration. The memory capacity is 2048 words of 16 bit length (referred to as a 2K x 16 memory). Physically, each bit plane consists of a 64 x 32 core matrix. Sixteen planes are mounted on a circuit board in a 4 x 4 arrangement. The memory functional layout is discussed in paragraph 4.

Memory Data Register (MDR): A 16-bit register which buffers all data to and from the memory. The contents of this register are also available to the Display Subsystem.

Memory Address Register (MAR): A 12-bit register which stores the address of the memory byte. Control of this register is also possible through the Display Subsystem.

Program Counter Register (PCR): A 12-bit register which contains the address of the next instruction to be executed. The least significant bit is always zero.

Accumulator (ACR): An 8-bit register which contains the data for the output bus and receives data from the input bus. It is also the primary arithmetic and logical register of the processor.

Cursor Register (CUR): A 12-bit register which controls the position of the cursor on the display. It can also be used in certain load, store, and arithmetic operations.

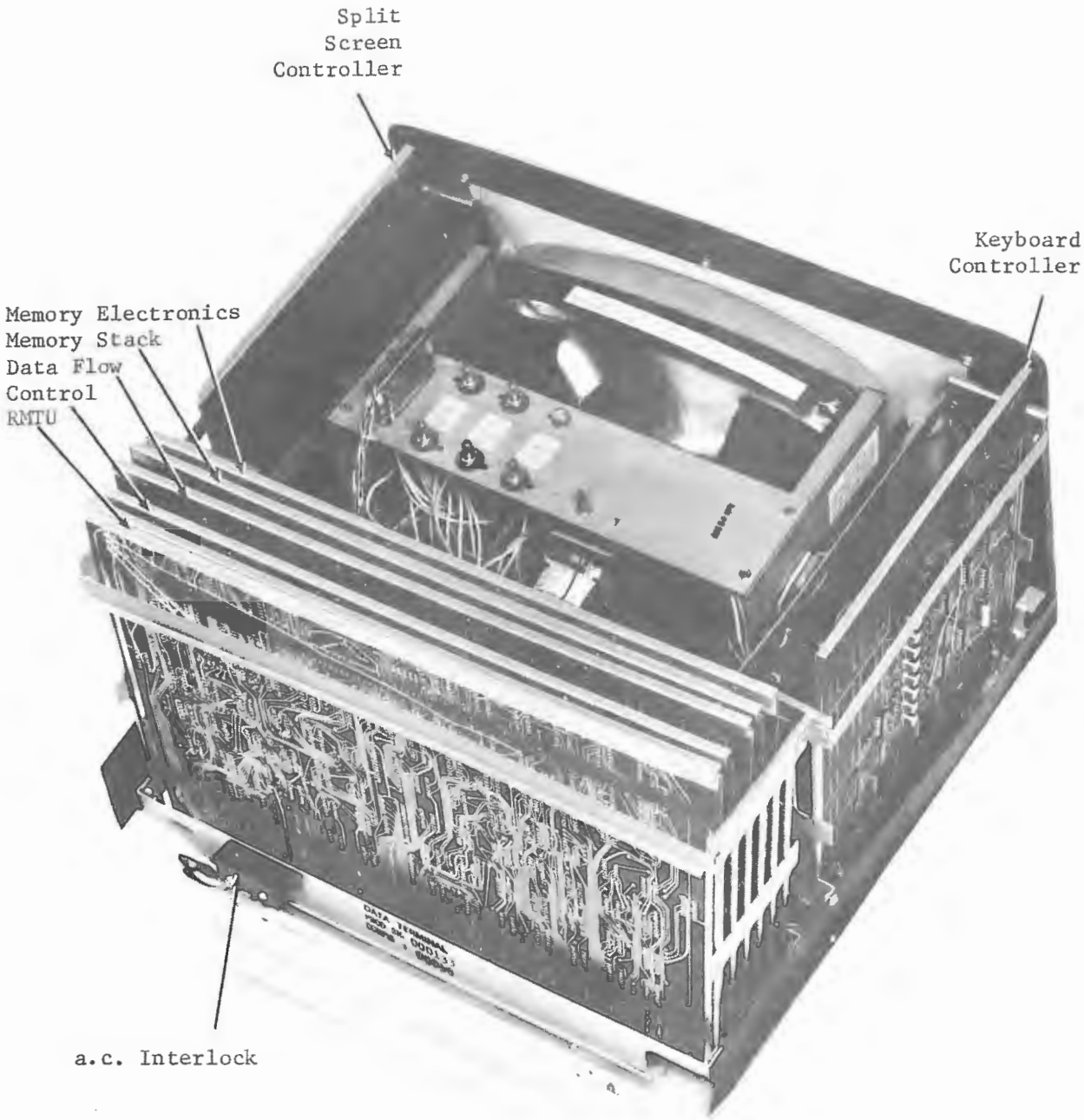
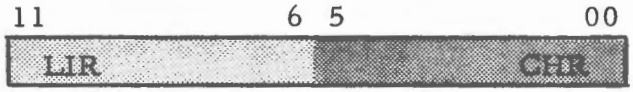


Figure 4-2. Circuit Board Identification and Location

Character Register (CHR): The least significant six bits of the cursor register which represents the cursor location on a line.

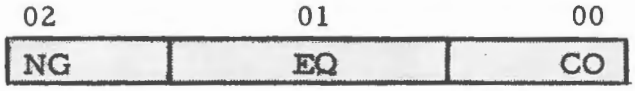
Line Register (LIR): The most significant six bits of the cursor register which represents the number of the line on which the cursor is displayed.



CUR

Cursor Register Layout

Condition Status Register (CSR): This 3-bit register stores the status of all arithmetic operations.



Negative (NG) ... Set if the most significant bit of the arithmetic unit (ARU) operation is 1.

Equal (EQ) ... Set if the result is zero after an Arithmetic Unit or Auxiliary Arithmetic Unit operation.

Carry Out (C) ... Set on an overflow condition from AAU or ARU operation.

Arithmetic Unit (ARU): This 8-bit unit performs arithmetic and logic operations such as add, subtract, and, or.

Auxiliary Arithmetic Unit (AAU): This 12-bit unit provides capability for +1, +2, +4, -1 and comparison operations on a word basis.

Input Data Bus (IDB): This 8-bit bus consists of eight lines which transfer data from an I/O device to the accumulator (ACR).

Output Data Bus (ODB): This bus consists of eight lines which transfer data from the accumulator (ACR) to an I/O device.

Peripheral Address Bus (PAB): This bus transmits the address and function command for a selected peripheral directly to the device. Sixteen lines are used for the address and four bits are

used to define the function to be performed by the peripheral device. The information is obtained as a decoded output from the Memory Data Register.

2. Control

The SPD 10/20 control electronics are contained on a single printed circuit board. Numerous control functions are provided by the interaction of system timing phases and extensive signal gating. A primary function is the decoding of the operation code and subsequent directing of the specified instruction. The State Counter and Real Time Clock are located on this board.

3. Refresh and Timing

The refresh and timing circuit board performs two major functions: one is the generation of a system timing chain; and the other is the processing and interfacing of data from the TPU to the CRT display. Circuits are provided to compute the CRT line number and character position on a line. The selected character is converted to a 7 x 10 dot matrix by the read-only memory which modulates the CRT video circuit and displays the character on the screen. The displayed character is refreshed at a rate that prevents image flickering.

4. CRT Display Unit

The CRT display is a commercially purchased (Sylvania) TV monitor. It is completely self-contained and has a viewing area that measures 9-1/2 inches wide by 7 inches high. In a single SPD 10/20 configuration, the display format consists of 30 lines of 64 characters each. In a dual SPD 10/20 configuration, both screens display 15 lines of 64 characters each.

4.2.3 Interface Control

Each communications line and peripheral device driven by the SPD 10/20 requires an associated controller to provide the interface between the external device and the TPU. Four standard controllers are available. Each one is self-contained on a plug-in printed circuit board.

The SPD 10/20 can accommodate a maximum of eight Controllers, all under TPU control. Table 4-1 lists the Controllers by type, function and external device controlled.

Table 4-1. SPD 10/20 Controllers, Related Functions and External Devices

Controller	Function	External Device
Keyboard	ASCII interface with SPD 10/20 keyboard. (Two required for auxiliary operation.)	Keyboard
Asynchronous	(EIA) Standard RS-232-C interface for communicating with standard line modems. One controller for half duplex. Two controllers for full duplex. Operation is 50 to 2400 Baud.	SPD-M Multiplexer, Data-speed Service, Teletype, TWX, Telex, Honeywell Data Station, SPD-P Printer, Remote Load.
Synchronous	(EIA) Standard RS-232-C interface for communicating with standard line modem. One controller for half duplex. Two controllers for full duplex. Operation is 1200 to 4800 Baud.	Univac DCT 2000, IBM 2780, RCA 70/740, Dataterm, Remote Load.
Split Screen	Used with Auxiliary Display to provide Master Display time sharing.	SPD Auxiliary Terminal.

4.3 ADDRESSING AND INSTRUCTION FORMATS

4.3.1 Introduction

The purpose of this paragraph is to provide a fundamental discussion of the addressing and instruction formats used with the SPD 10/20 Terminal. Refer to the SPD 10/20 Programmers' Reference Manual for a detailed discussion of this subject plus a complete listing of instruction formats, operation codes and hexadecimal function codes.

4.3.2 Hexadecimal Notation

In programming the SPD 10/20, memory addresses and instruction codes are listed in the hexadecimal notation. It is a convenience, like shorthand, to express a code as four hexadecimal symbols rather than a string of 16 binary symbols (1's and 0's).

Any positional number system can be defined by its base (radix). The base is the number of unique symbols that can occupy a position in the number system. For example, the binary system has two symbols (base 2); the octal system has eight symbols (base 8); and the decimal system has ten symbols (base 10). The hexadecimal system has 16 symbols, so it is a base 16 system. The symbols are: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F (see Table 4-2).

Table 4-2. Decimal, Binary and Hexadecimal Equivalents

Decimal	Binary	Hexadecimal	
		Symbol	Spoken
0	0000	0	Zero
1	0001	1	One
2	0010	2	Two
3	0011	3	Three
4	0100	4	Four
5	0101	5	Five
6	0110	6	Six
7	0111	7	Seven
8	1000	8	Eight
9	1001	9	Nine
10	1010	A	Able
11	1011	B	Baker
12	1100	C	Charlie
13	1101	D	Dog
14	1110	E	Easy
15	1111	F	Fox

In converting from hexadecimal to decimal, the symbol represents both a coefficient and its position in the number (the exponent of the base). The exponent of the base (position) is determined by counting from right to left. For example, convert the hexadecimal number 4F2 to its decimal equivalent. Refer to Table 4-2 for the value of symbol F.

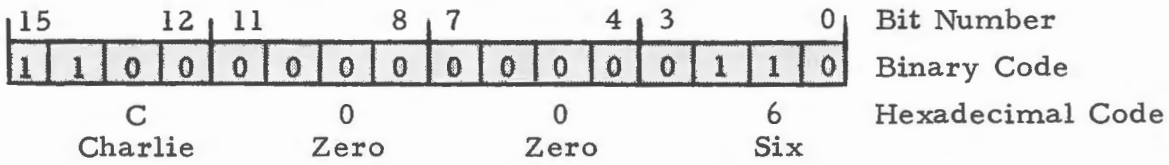
$$4F2 = 4(16^2) + F(16^1) + 2(16^0)$$

$$= 4(256) + 15(16) + 2(1)$$

$$= 1024 + 240 + 2$$

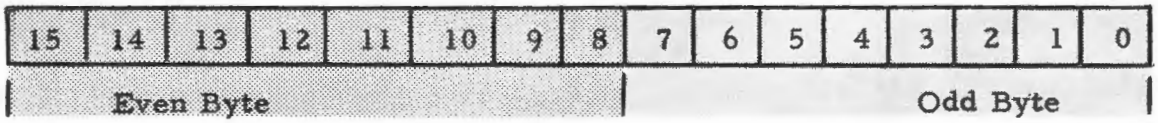
$$= 1266$$

The Enable Interrupts (ENB) instruction is presented as an example of the convenience of coding in the hexadecimal system.



4.3.3 Word Formats

The SPD 10/20 addressing and instruction word is composed of an odd/even byte pair, containing eight bits each. The word can be accessed by addressing either byte; however, for compatability, the address of the even byte should be used.



16 BIT WORD

There are three major instruction formats:

1. Non-memory reference
2. One word memory reference
3. Two word memory reference.

1. The non-memory reference instructions are a group of operations which contain their own data; therefore, they do not need to request data from memory. The non-memory reference data is made up of an op code and data which instructs the Terminal to operate on what is supplied in that data word.

2. The one word memory reference is an instruction in which a particular location in memory is fetched during the instruction cycle. If the resulting data is determined to be the effective data, the Terminal will operate on it during the execute cycle.

3. The two word memory reference only occurs when test jumps or test input-output is desired. The data is arranged such that the first word is used for operating instructions while the second contains address information.

4.3.4 Instruction Classes

The SPD 10/20 provides a repertoire of 58 instructions including:

16 data manipulation
11 cursor control
20 test and/or branch
6 input/output
4 miscellaneous

1. Byte Class: An op code instruction dictating action on the byte at the effective address. Actions are:

Load	Store	Add	Subtract
Compare	And	Or	

2. Cursor Class: The data in the cursor register (line and character taken together) can be loaded with the word at the effective address, stored at the effective address, or compared to the effective address.

3. Increment Class: The word at the effective address can be incremented by one, incremented by two, or decremented by one.

4. Jump Class: Provides for an unconditional jump to the effective word address or jump to a subroutine, in which case a return address is stored.

5. Test Jump Class: A test jump is two words long; the first contains operating data, the second contains address data. This instruction is conditional.

6. Immediate Class: The effective data is located in the odd byte of the instruction word.

7. Input/Output Class: Provides device attention to I/O controllers and provides the necessary interface select and enabling data. Included in this class are Control, Read and Write with a conditional test for possible jump.

8. Operate Class: Enables a large majority of data movement within the Terminal's operating registers. Interface commands also form a part of this class.

4.3.5 Effective Address Calculation

An example of an effective address calculation is presented in this paragraph. The textual discussion is supported by diagrams of the instruction words.

Prior to the discussion, it is necessary to explain the functional division of the core memory. Figure 4-3 shows the functional division of a memory bit-plane. Each plane contains 2048 locations (words). Information is transferred in and out of the memory as complete 16-bit words: that is, the identical core location in all 16 bit-planes. The memory is divided into eight sectors, each of which contains 256, 16-bit words or 512 bytes. Each sector is divided into an upper page and lower page of 128 words each. The highest numbered sector (7) is labeled TOP; sector 6 is labeled TOP-1. A 44 byte reserved area is contained in sector 7. Hex bytes 000 through 77F are reserved for refreshing displayed data. The remaining area is used for program storage.

A discussion of a sample effective address calculation is presented below. The text is keyed to Figure 4-4 which shows the layout of the one-word memory reference instructions used in the operation. Bit identification is as follows:

Bits 11 through 15:	Opcode
Bits 00 through 08:	Displacement (relative address) with defined sector
Bit 10:	Indirect addressing (0 = direct, 1 = indirect)

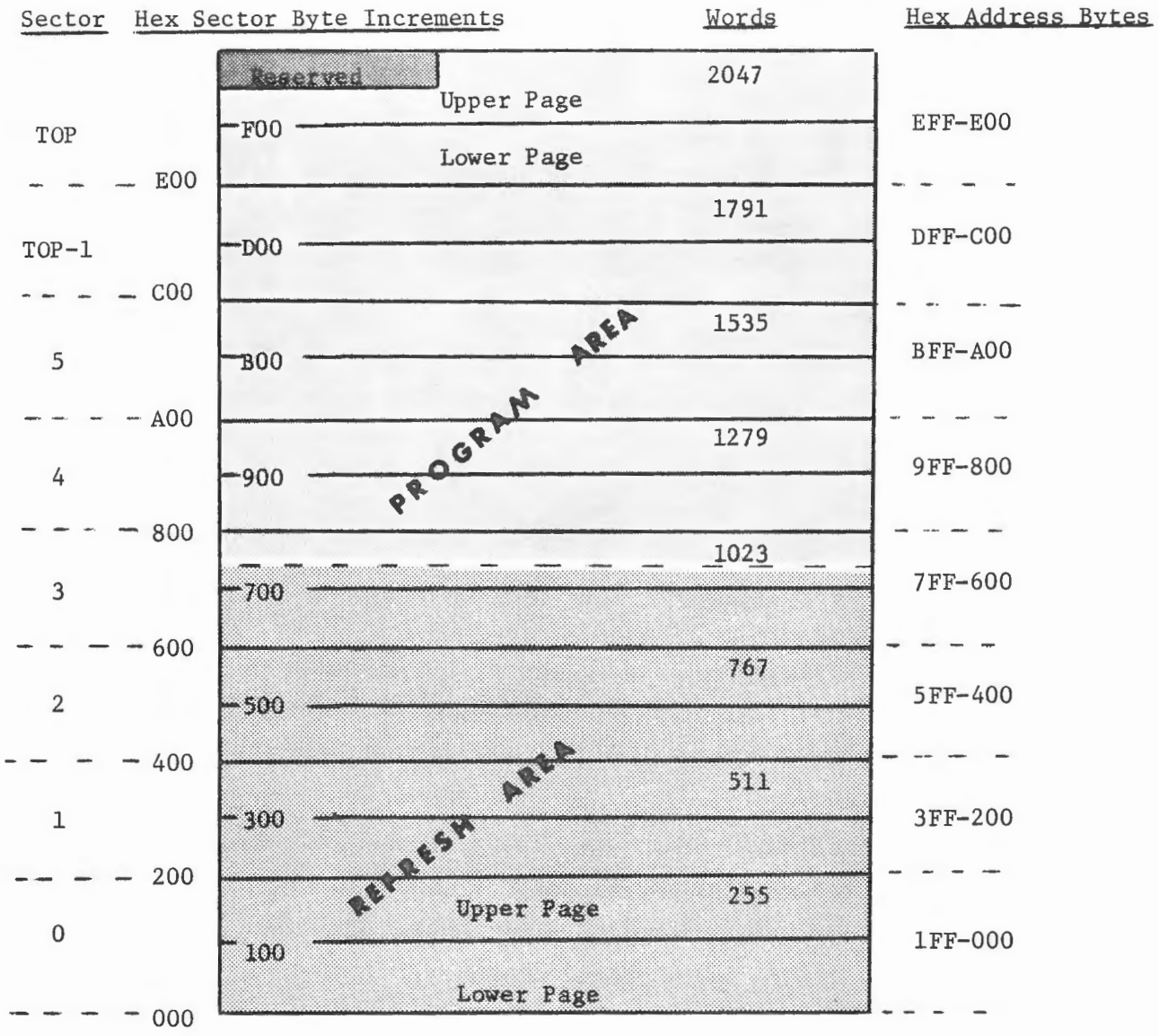


Figure 4-3. 2K Core Memory Layout

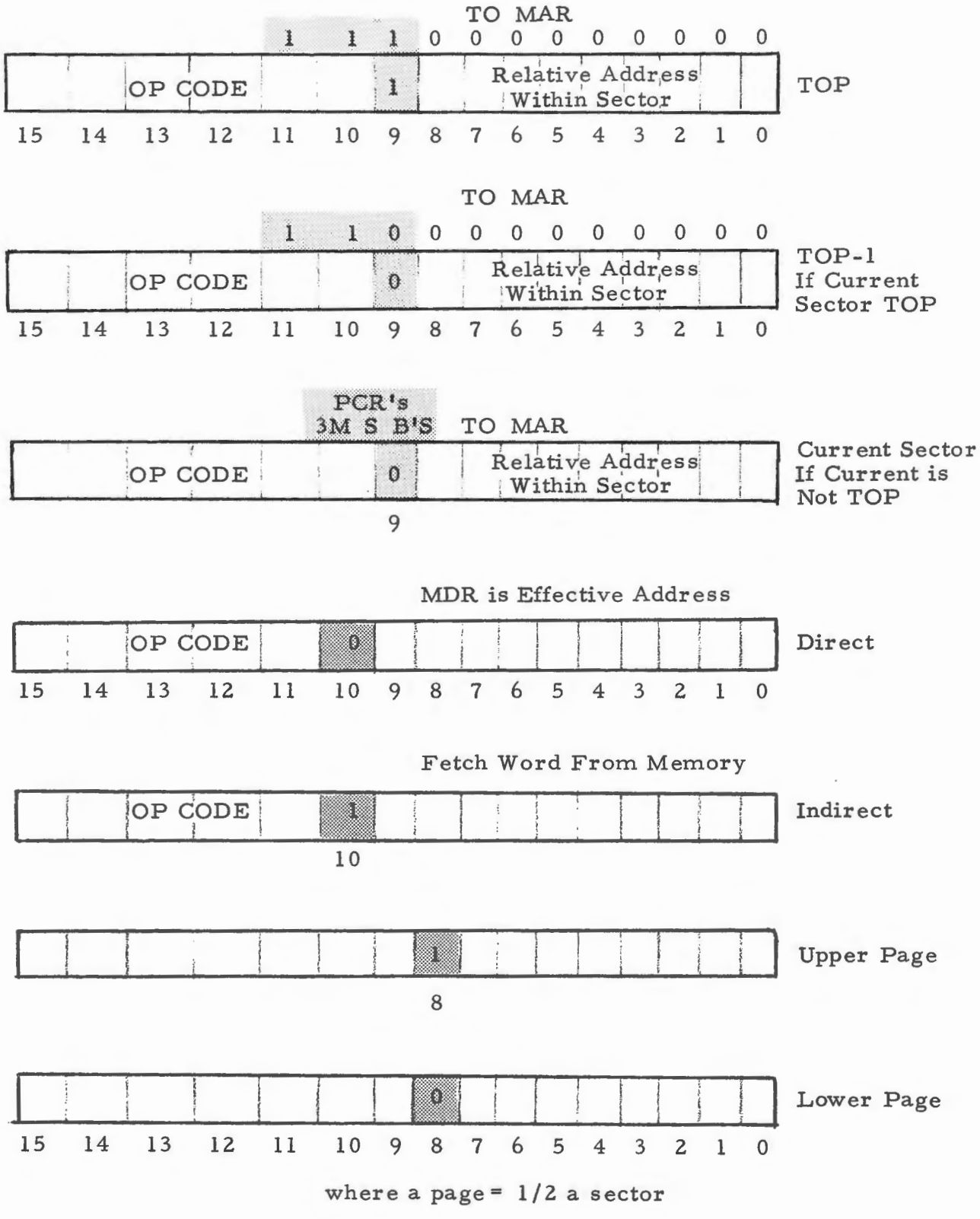


Figure 4-4. Effective Address Calculation Illustrated

Bit 9:	Sector address 1 = TOP sector 0 = Current sector if current sector ≠ TOP 0 = TOP-1 sector if current sector = TOP
Bit 8:	Page identification (0 = Lower page, 1 = Upper page).

Sample Effective Address Calculation (See Figure 4-4)

1. The sector bit (bit 9) is tested. If it is 1, the last sector of memory (TOP) has been referenced. The address of the top sector, linked with the instruction's displacement field, is loaded into the Memory Address Register (MAR). GO TO step (4).

2. If the sector bit is not 1, test to see if the current sector is TOP. If so, the sector below TOP has been referenced (TOP-1). TOP-1 linked with the instruction's displacement field is loaded into the MAR. GO TO step (4).

3. If the current sector is not TOP, then the current sector has been referenced. Combine the sector bits of the Program Counter (PCR) with the instruction's displacement and load the result into the MAR. Note that the PCR still contains the address of the current instruction at this point.

4. The indirect bit (bit 10) is tested. If it is 0, there is no indirect addressing, and the MDR contains the true effective address. The instruction execute cycle is entered which uses this address. The least significant bit (LSB) of the effective address has been maintained for use in byte instructions.

5. Indirect addressing is indicated. The MAR is used to fetch an indirect address word from memory, which is loaded into the MDR. If the indirect bit (bit 15) of this word is 1, continue by a GO TO step (5). If it is 0, the MDR contains the true effective address. The instruction execution cycle is entered, which uses this address. The LSB of the effective address has been maintained for use in byte instructions.

4.3.6 Basic System Timing and Data Flow

The system timing is generated on the Refresh Module and Timing Unit circuit board. The system operates on two cycles, each of which is divided into 20 equal increments or timing phases. The instruction cycle is first, followed by the execute cycle. During the instruction cycle, an instruction

is fetched during timing phases 1 through 10 and decoded during timing phases 11 through 20. During the execute cycle, the selected data is fetched during timing phases 1 through 10 and is operated on during timing phases 11 through 20.

The processing of a specific instruction (Increment and Store) is presented as a typical example of system activity with respect to timing. Obviously, each instruction requires a different data path within the TPU; however, some operations follow the same pattern, such as Memory Data Register strobe at time T4 and Program Counter Register update at time T19.

Processing of Increment and Store Instruction

The purpose of an Increment and Store instruction is to retrieve data in a specific memory location, add 1 to it, and return it to the memory. Figure 4-5 is a timing diagram for this operation.

Activity starts at time T4 when a memory data word is strobed into the Memory Data Register (MDR). At the trailing edge of T5, the opcode portion is decoded and saved in the Instruction Register so that during the remainder of the operation the computer knows what it is supposed to do. The address portion of the word is taken from the MDR and after T11, enabled to the Auxiliary Arithmetic Unit (AAU) where zero is added to it, and it is loaded into the Auxiliary Arithmetic Register (AAR) at T17. At T19, the address is placed in the MAR, such that the MAR is pointed to the address which it is desired to increment. At this point, the instruction cycle has been performed and the execute cycle is entered.

Execute cycle time T4 enables the MAR Selected Data from the MDR to the Auxiliary Arithmetic Unit where it is incremented by one, and at T7, the result is placed in the Auxiliary Arithmetic Register. Also at T7 the CSR is set as required. At T9, the AAR data is placed in the MDR so that it can be written back into memory. The line and character are not important unless a cursor operation is involved. At this point, the data movement called for has been performed. All that remains is to up-date the Program Counter Register (PCR). After T11, the PCR is enabled to the Auxiliary Arithmetic

Unit where a +2 is added to it (+2 because of byte orientation, two bytes per word). At T17, it is enabled to the Auxiliary Arithmetic Register. At T19 the PCR and MAR are updated, which finishes the operation.

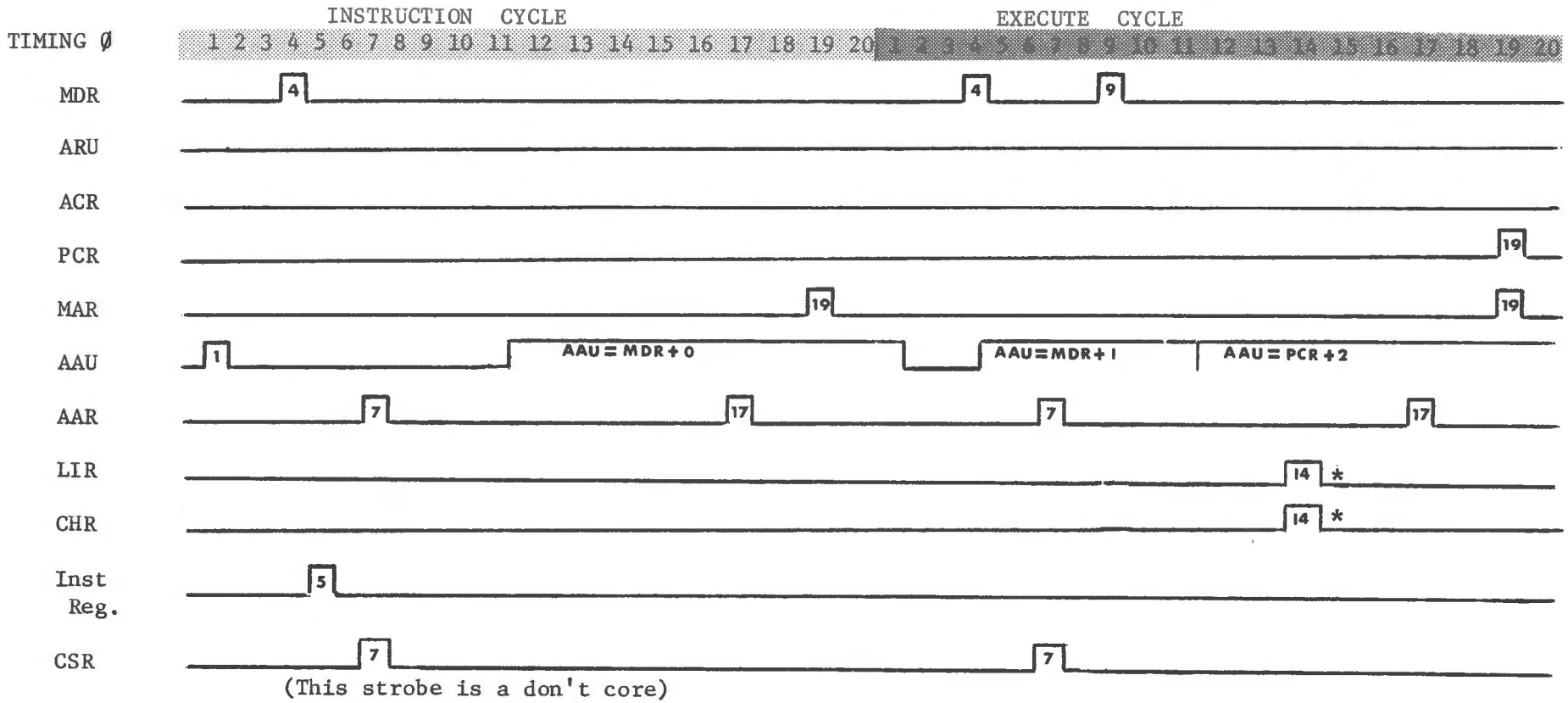


Figure 4-5. System Timing Example, Increment and Store Instruction

CHAPTER V

THEORY OF OPERATION

5.1 LOGIC UTILIZED

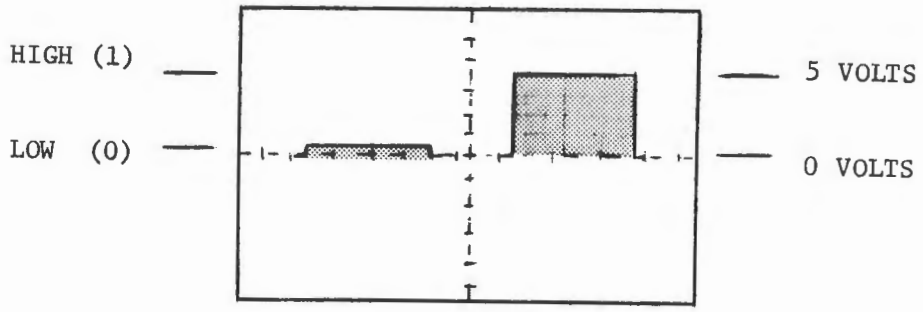
The INCOTERM SPD family of products uses only proven Integrated Circuits. The large majority are Texas Instruments 7400 Series Transistor Transistor Logic (TTL), sometime called (T^2L). Package sizes utilized include the 14, 16 and 24 pin dual in line, meaning an equal number of pins located on either side of the package. Figure 5-1 illustrates the pin numbers and package indexing. Table 5-1 provides a comprehensive listing of the logic utilized with reference to the appropriate Texas Instruments catalog pages.

5.1.1 Logic Levels

When discussing the theory of operation, digital logic terminology is frequently used. What this means is that positive logic levels can be referred to in two ways:

1. a logical 0 (zero) will be called either 0 (zero) or a low.
2. a logical 1 (one) will be called a 1 (one) or a high.

With respect to voltage, a typical logic 0 output is in the neighborhood of 0.2 volts and a logic 1 is between 3.5 and 5 volts. Graphically, the above levels will look like this:



Another term encountered is TRUTH. The Truth of a device is defined as the output level resulting from a predetermined combination of inputs. Schematic symbology used to indicate device operating conditions, tell the technician when a device output is true. The following are simple examples. A listing of truths for all incorporated devices is unnecessary and repetative. The Texas Instruments catalog should be referenced. Example A illustrates NAND and OR gates with device operation defined by the Truth Table.

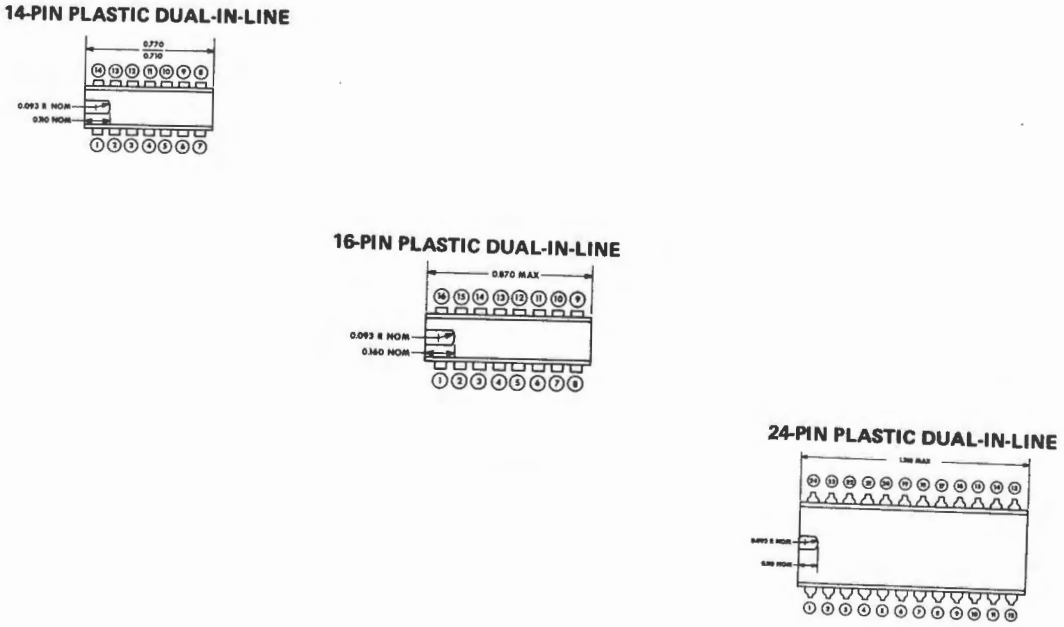


Figure 5-1. Integrated Circuit Pin Identification

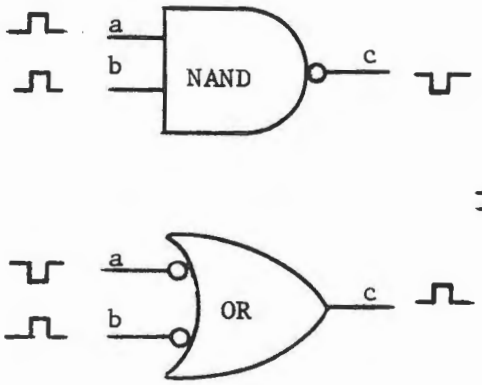
Table 5-1. Integrated Circuit Reference Table

Item	Catalog Sec-Page	Description	Designation	Remarks
1.	2-5	ICSN7400	A00	Quad. 2 Input Pos. Nand Gate
2.	2-9	ISCN7402	A01	Quad. 2 Input Pos. Nor Gate
3.	2-10	ICSN7403	A02	Quad. 2 Input Pos. Nand w/Open Col.
4.	2-11	ICSN7404	A03	Hex Inverter
5.	2-12	ICSN7405	A04	Hex Inverter w/Open Col.
6.	2-13	ICSN7410	A05	Triple 3 Input Pos. Nand
7.	2-14	ICSN7420	A06	Dual 4 Input Pos. Nand
8.	*S2-15	ICSN7426	A07	Quad. 2 Input Hi. V. Interface Nand
9.	2-15	ICSN7430	A08	8 Input Pos. Nand
10.	2-16	ICSN7440	A09	Dual 4 Input Pos. Nand Buffer
11.	5-7	ICSN7442	B00	4 Line to 10 Line Decoder (1 of 10)
12.	2-17	ICSN7451	A12	Exp. Dual 2 Wide 2 Input and/or Invert.
13.	2-19	ICSN7454	A13	Exp. 4 Wide 2 Input and/or Invert.
14.	2-26	ICSN7472	A14	J-K Master-Slave Flip Flop
15.	2-32	ICSN7474	A15	Dual J-K M-S F/F w/Preset & Clear
16.	6-1	ICSN7475	B01	8 Bit & 4 Bit Bistable Latches
17.	2-35	ICSN7476	B02	Dual J-K Master Slave F/F
18.	7-19	ICSN7483	B04	4 Bit Binary Full Adder
19.	7-27	ICSN7486	A16	Quad 2 Input Excl. -Or
20.	8-1	ICSN7490	A17	Decade Counter
21.	8-13	ICSN7493	A18	4 Bit Binary Counter
22.	9-25	ICSN7495	A19	4 Bit Right-Shift Left-Shift Reg.
23.	6-1	ICSN74100		8 Bit & 4 Bit Bistable Latches
24.	5-13	ICSN74145	B05	BCD to Decimal Decoder/ Driver
25.	*S5-7	ICSN74154	CC0	4 Line to 16 Line Decoder/ Driver
26.	3-17	ICSN74H40	A10	Dual 4 Input Pos. Nand Buffer
27.	3-40	ICSN74H76	B03	Dual J-K Master Slave F/F
28.	4-5	ICSN74L04	A11	Hex Inverter
29.		ICSN7524	(x) B06	Sense Amplifier
30.		ICSN75324	(+) A20	Memory Driver w/Decode Inputs
31.	11-1	ICSN74180		8 Bit Odd/Even Par. Gen. / Checker
32.		F9601/NS7026	(-)	Retriggerable Monostable Multivibrator
			(x) B06	T. I. Bulletin No. SC 10452
			(+) A20	DL-S69 11169
		F9601/NS7026	(-)	See Fairchild Bulletin

NOTE: T.I. CATALOG NOS.
CC 201-R

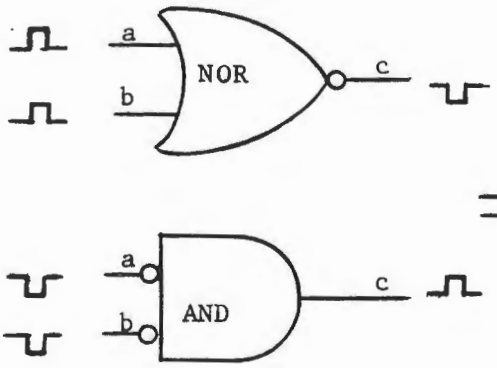
*Suppl. CC 301

Verbally, the output c will be high if either input (a OR b) is low (true), but not when both a and b are high.



a	b	c
0	0	1
0	1	1
1	0	1
1	1	0

Example A

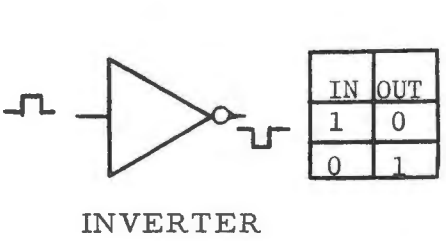


a	b	c
0	0	1
0	1	0
1	0	0
1	1	0

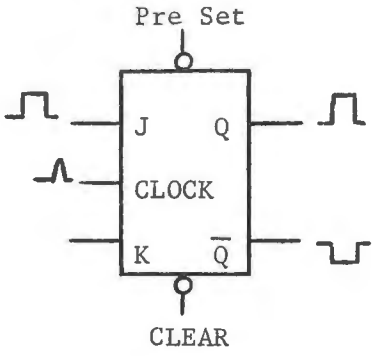
Example B

Definition: The circular symbol at either the input or output denotes a Logical Zero (0) is required. Conversely, if a circle is not present, a 1 (high) is indicated.

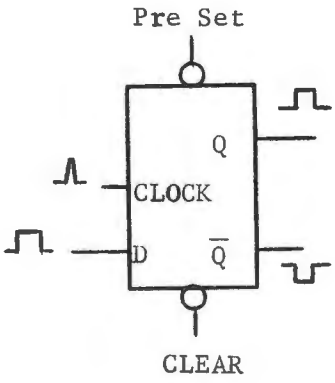
Example B gates are the inverse of example A gates and are called NOR and AND gates. In operation the gates will produce a true output opposite to example A functions. The SPD 10/20 uses an intermix of both High and Low Truth, which takes advantage of the functional operation illustrated in both examples. Some other schematic representations are:



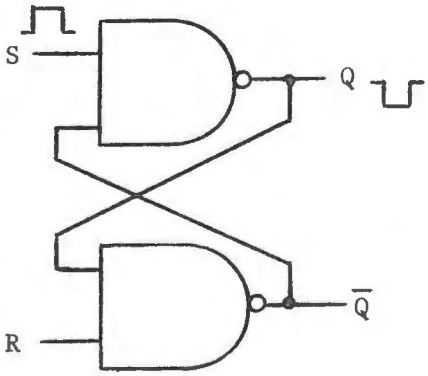
IN	OUT
1	0
0	1



IN	OUT
JK	Q $\overline{Q}$
0 0	Q $\overline{Q}$
0 1	0 1
1 0	1 0
1 1	$\overline{Q}$ Q



IN	OUT
D	Q $\overline{Q}$
0	0 1
1	1 0

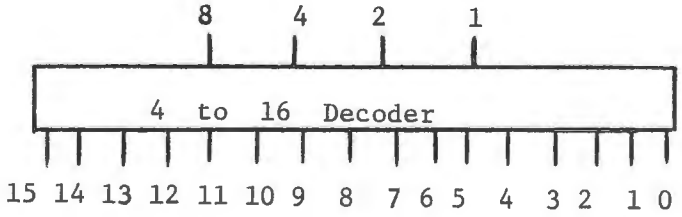


S R	Q
0 0	---
0 1	1
1 0	0
1 1	N/C

Preset and clear are not dependent on the clock
preset = Low set Q High
clear = Low sets Q Low

5.1.2 Schematic Interpretation

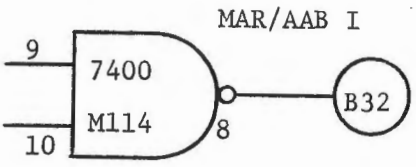
Obviously the above examples are not inclusive of all data presented on the schematics. However, even the most complex IC's are represented by a box with its functional notation and pin connections. An example of this may be a four to 16 decoder which is easily represented as follows:



When using the schematic for the purpose of tracing logic signal flow, the procedure is described as follows:

Condition 1 - the signal is terminated at the circuit board connector.

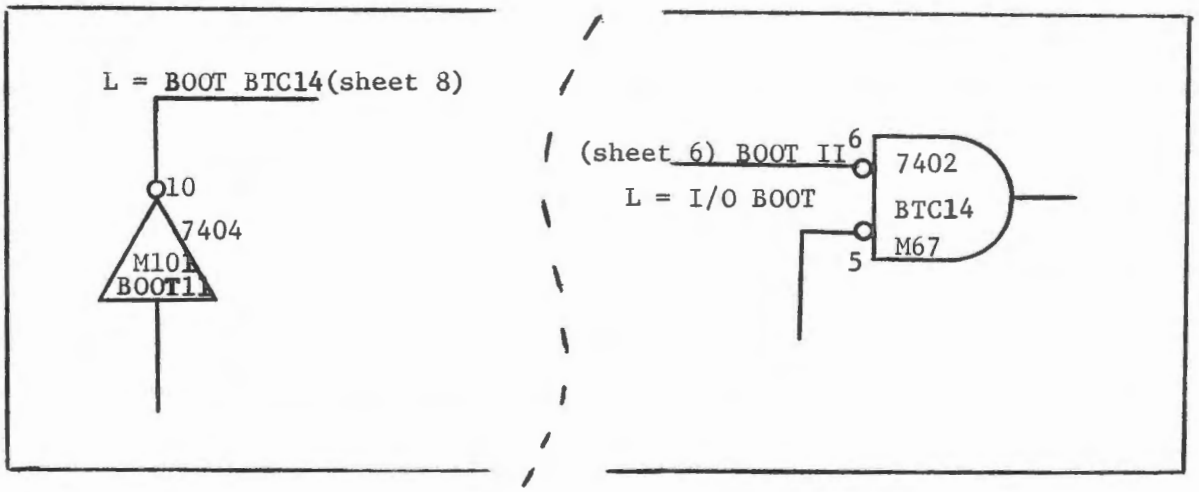
EXAMPLE



Explanation - The numbers located within the gate provide the IC device type (7400) and the physical location (M114). Each IC has an M number which can be referenced to a circuit board layout and pinpoints its physical location. The pin numbers are provided as indicated, inputs are 9 and 10 and output is Pin 8 (notice it is low truth). The gate function indicates a Memory Address Register to Auxiliary Arithmetic Bus data transfer. The I on the end indicates this is an inversion of the MAR/AAB signal. The reason for the inversion is to provide a Low because the AAB is a low truth bus. The B32 within the circle is the connector pin on which the signal is leaving the circuit board. There are two connectors per board, A and B, each consisting of an 86 pin receptacle. In tracing the signal to its destination, the physical board location number must be known. In this case the IC illustrated, is on the control board, which is located in position 13 (see Chapter 2). Referring now to the large connector wiring list print No. 005-10-30, there are two ways the information can be looked up. One is to scan through the net signal name until finding MAR/AAB I. The second is to look for B 13 32 (connector B, Slot 13 and Pin 32 respectively). The resulting look-up locates the signal on Sheet 12 and indicates that the signal is wired to B 12 09 (connector B Slot 12 Data Control Pin 9). The final step is to locate on the Data Flow Schematic, the circle with B9 in it, which will lead to the signal destination.

Condition 2 - signal flow remains on the same board but is on another sheet of the schematic.

EXAMPLE



Explanation - the example illustrates a signal which originates on the data control schematic sheet 6 (left illustration). The nomenclature is similar to condition 1 except the device function. In this case it is BOOT II, which stands for a Boot signal with double inversion. The termination on Print 6 indicates the signal goes to Sheet 8. For the purpose of tracing flow, the L = Boot can be ignored. The BTC 14 is the designation for the device to which the signal will flow. On the right side of the illustration it can be seen that if the signal route had been reversed, i. e., it was desired to see where the input to Pin 6 M 67 came from. The sheet and device are provided which indicate that the signal came from Pin 6 device designated BOOT II. The above examples are simple cases and provided only for familiarization. In actual practice, a large portion of signals flow to more than one point and the flow from the initial signal, through functional gating and to its ultimate destination, can become quite lengthy.

5.2 DATA FLOW ELECTRONICS

5.2.1 Introduction

All the data flow electronics are contained on one printed circuit board located in slot 12. It contains all the registers and associated gating to provide signal steering, buffering and driving. Refer to paragraph 4.2.2 and Figure 4-1 for a brief description of each register and its functional relationship in the system. The major functional units are listed below.

1. Register Clock Drivers
2. MDR-to-ACR Exclusive Or Unit
3. Memory Data Register (MDR)
4. MDR Data Bus
5. Memory Data Bus Drivers
6. Memory Address Register (MAR)
7. Memory Address Bus
8. Arithmetic Unit Adder
9. Arithmetic Unit Bus
10. Auxiliary Arithmetic Unit Adder
11. AAU Bus
12. AAU Register
13. AAU Operand Steering
14. Character Register (CHR)
15. CHR Steering
16. Line Register (LIR)
17. LIR Steering
18. Accumulator Register
19. Condition Status Register (CSR)
20. Program Counter Register (PCR)
21. Test Comparator

22. MDR Bus Enable Decoders

23. Register Enable Drivers

A simplified block diagram of the data flow electronics is shown in Figure 5-2. Detailed logic diagrams are referenced in drawing 001-02-01 (34 sheets). A photograph of the component side of the board is shown in Figure 5-3.

5.2.2 General Discussion of Data Flow

This general discussion is referenced to the block diagram shown in Figure 5-2.

The Memory Data Register (MDR) is a 16-bit register that buffers all data to and from the memory, which contains 2048 16-bit words. The MDR can be enabled to the Arithmetic Bus (ARB) to provide data to the Arithmetic Unit Adder which outputs to the Accumulator Register (ACR). The ARB, ARU and ACR can handle only 8-bits so these data transfers consist of bytes rather than words. The ACR can send data back to the MDR in 8-bit bytes, which means it can fill either half of the memory word (odd or even byte).

Memory address selection utilizes the 12-bit Memory Address Register (MAR). The MAR addresses 4096 bytes (2048 words).

The SPD 10/20 contains a complete 12-bit arithmetic path that includes the Auxiliary Arithmetic Unit Adder, Register, Bus and Operand Steering. The AAU is not a general adder but it does perform+ 4, +2, +1, -1 and compare operations. The AAU can be enabled to the MAR, PCR and Cursor Register (CUR). The CUR is composed of two 6-bit registers: the Line Register (LIR) and the Character Register (CHR). The MAR, MDR, PCR and CUR can feed back into the AAU. Arithmetic operations can be performed by the AAU on data from these registers.

The CUR can also be considered as a unit of the byte (8-bit) arithmetic path which utilizes the ARU and ACR. In this situation, its components must be considered separately; that is, the 6-bit LIR or the 6-bit CHR.

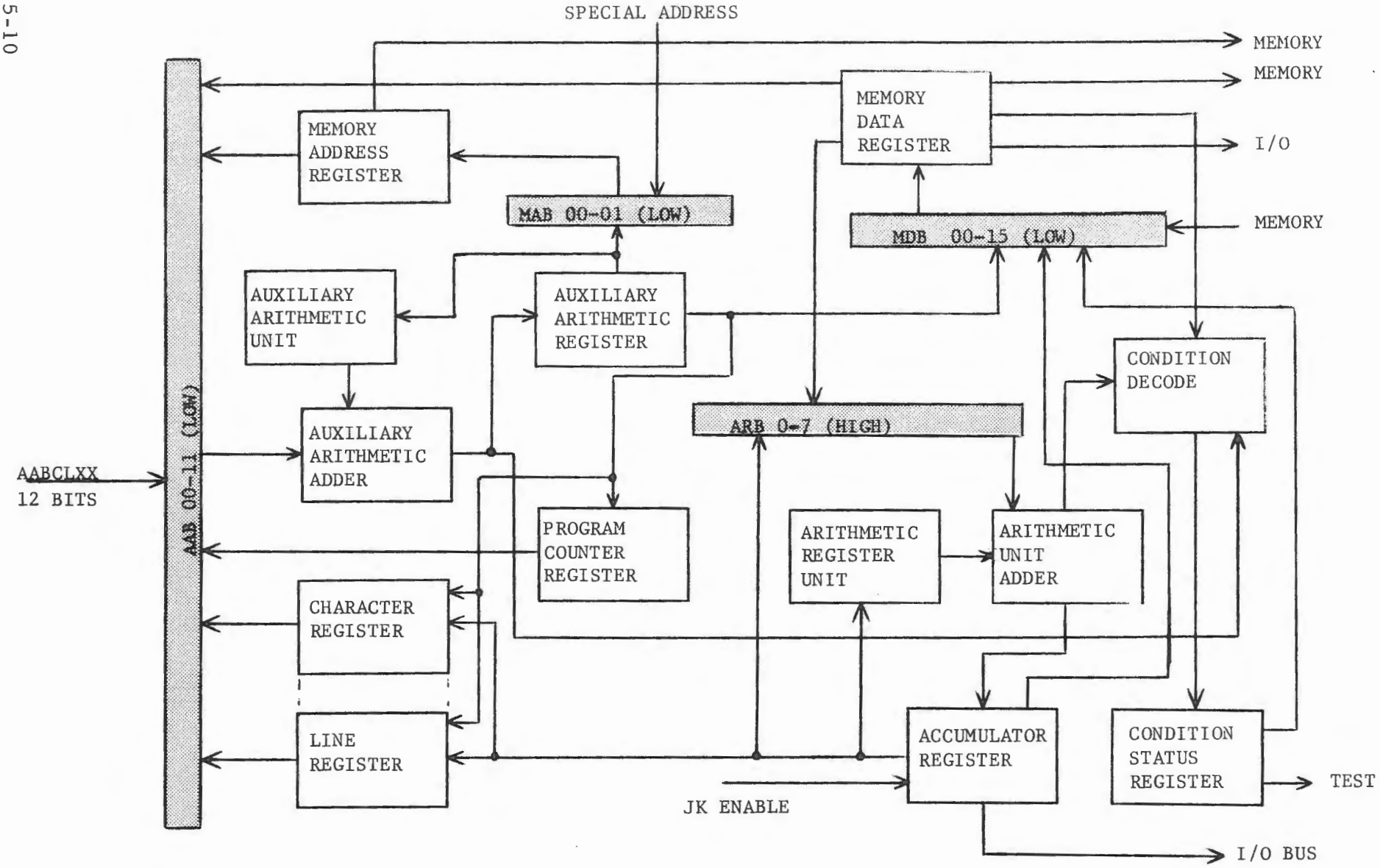


Figure 5-2. Simplified Block Diagram TPU Data Flow

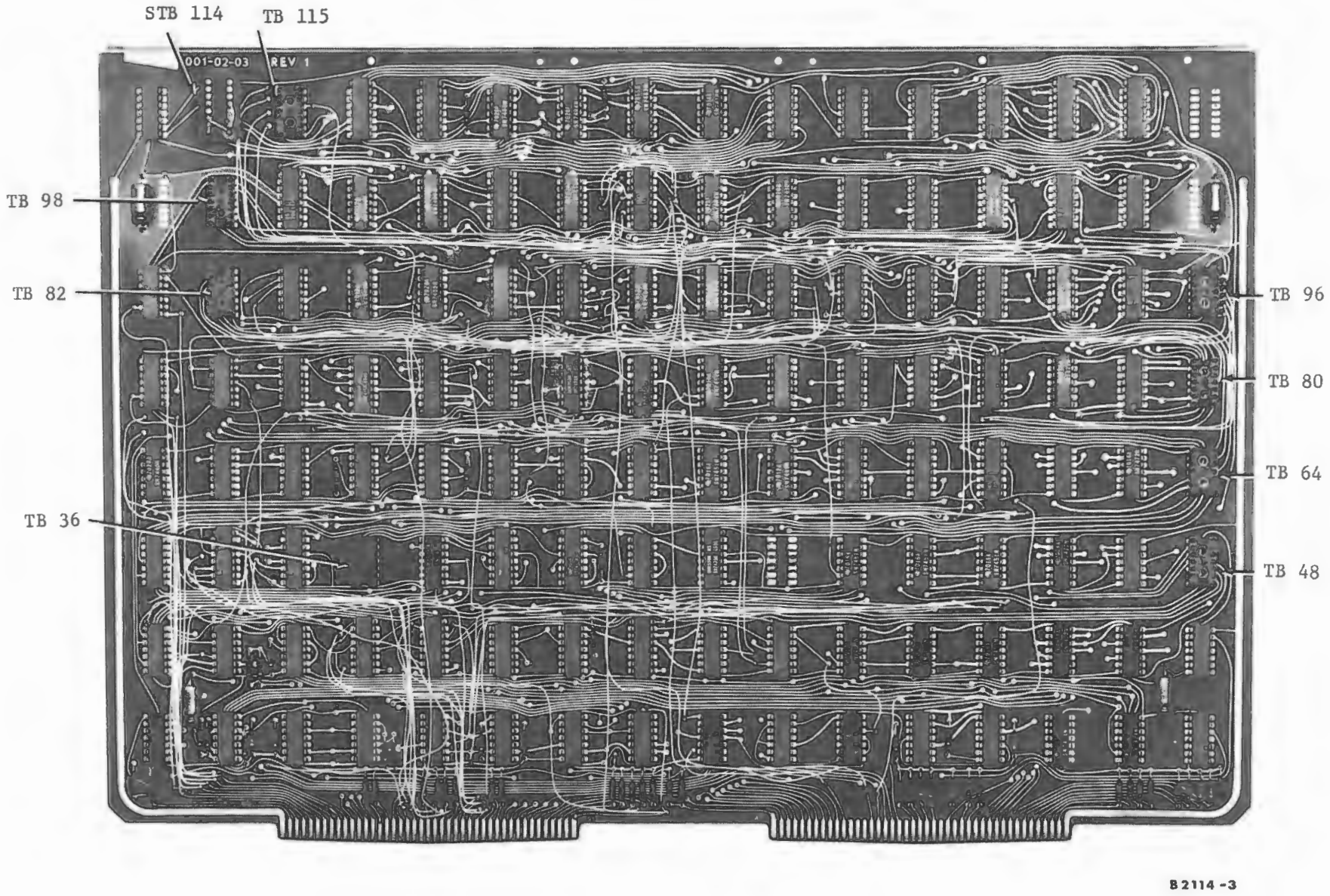


Figure 5-3. Data Flow Module

5.2.3 Bus System

Data flow between registers is accomplished on buses (see Figure 5-2). Four buses are used and are identified as follows:

Memory Data Bus	(MDB)	- 16 bits
Memory Address Bus	(MAB)	- 12 bits
Arithmetic Bus	(ARB)	- 8 bits
Auxiliary Arithmetic Bus	(AAB)	- 12 bits

The ARB is high truth and the others are low truth.

The input to the Memory Data Register comes from the Memory Data Bus. The inputs to this bus are the memory, AAU register, ACR (either byte) and CSR. Data from the CSR is the result of an arithmetic operation. The CSR is a 3-bit register that stores the status of all arithmetic operations. Its contents indicate conditions of Carry Out, Equal or Negative.

From the MDR, data can be enabled to the Arithmetic Bus (odd or even byte), Auxiliary Arithmetic Bus or the Condition Store Register.

5.2.4 Memory Address Register

The Memory Address Register (MAR) is a 12-bit register that stores the address of the memory byte. The logic for the MAR is shown on sheets 10 and 11.

The register consists of three 4-bit bistable latches (type 7475) that are synchronously clocked by signal MARCLK. The input to the MAR is the 12-bits from the Memory Address Bus (MAB00-MAB11). The Q and $\overline{Q}$ outputs from each latch are sent to the Memory Electronics board. The $\overline{Q}$ output of each latch is also connected to one input of an Auxiliary Arithmetic Bus driver (M40, M17 and M33). The other input of each driver is connected to enabling signal MAR/AAB which transfers the data from the MAR to the AAB.

Outputs MAR01*-MAR10* are connected to gates M37 and M103 which are shown on the left side of sheet 11. This logic is used to obtain the address of the Cursor. The last word of memory (hex FFE for a 2K system) is reserved for the Cursor. An address, rather than an instruction, is used to reference the 12-bit Cursor Register. M90 (MARCUR) generates the signal when it is

enabled (high). M37 (MAD11) and M103 (MAD10) are nand gates that are connected to the inputs of M90. When all the inputs to M37 and M103 are high, M90 is enabled.

5.2.5 Arithmetic Unit Adder

The Arithmetic Unit Adder (ARU) is the byte (8-bit) arithmetic unit. It performs arithmetic and logic operations such as add and subtract. Refer to sheet 14. It consists of two type 7483 4-bit binary full adders (M126 and M127) and two type 7402 quadruple 2-input positive nor gates (M95 and M110). Gates M95 and M110 are shown symbolically as negated input and gates which are logically equivalent to positive nor gates (reference paragraph 5.1). This configuration adds two 8-bit binary numbers and produces the resultant carry from the eighth bit. For each 4-bit adder (ARA00-03 and ARA04-04), the A-inputs are for one 4-bit input number and the B-inputs are for the other. Each of the B-inputs (eight total) has an input gate (M95) connected to it. The enabling signal ACR/ARU is sent to one input of every M95 gate; the other input is a bit from the Accumulator Register (ACR00* through ACR07*). The A-inputs to the adders are connected to the Arithmetic Bus (ARB00 through ARB07). If the adders are not enabled, the circuit performs like a steering network. For example, the byte being operated on is enabled to the ARB and then to the ARU. In the disabled condition (ACR/ARU high), a zero is added to the byte and it is enabled to the ACR.

5.2.6 Arithmetic Unit Bus

The Arithmetic Unit Bus (ARB) is shown on sheet 15. It contains inputs from the Exclusive-Or Unit, Memory Data Bus Drivers, Character Register, and the Accumulator Register. A set of gates (M12 and M16) accept the eight input bits (INB00 through INB07), inverts them and enables them to the Arithmetic Bus.

5.2.7 Auxiliary Arithmetic Unit

The Auxiliary Arithmetic Unit (AAU) is composed of the following major functional components. Sheet numbers for the associated logic diagrams are also shown.

1. Adder (sheet 16)

2. Auxiliary Arithmetic Bus (sheets 17 and 18)

3. Register (sheets 19 and 20)

4. Operand Steering (sheets 21 and 22)

The AAU adder is a 12-bit unit that performs +1, +2, +4, -1 and Compare operations. It consists of three type 7483 4-bit binary adders (M116, M117 and M120) and two type 7404 hex inverters (M118 and M119). The adders are interconnected to provide adding of two 12-bit binary numbers and generation of the resultant carry from the 12th bit. The A-inputs of the adder are for one 12-bit number and the B-inputs are for the other. The B-inputs are taken directly from the outputs of the steering network and are identified as AAD00 through AAD11. These signals determine the operation to be performed; that is, +1, +2, etc. The A-inputs are taken from the Auxiliary Arithmetic Bus and are inverted before they are applied to the adder. These signals are identified as AAB00 through AAB11. The adder outputs are sent to the AAU Register.

The Auxiliary Arithmetic Bus (sheets 17 and 18) accepts inputs from the Memory Data Register, MAR, CHR, LIR, and PCR. A nand gate is connected to AAB11, -10 and -9. A high LOW/AAB signal, which is common to all three gates, forces these three bits to a logical 1. As previously stated, the outputs from the AAB are sent to inverters in the B-input lines of the adder.

The AAU Operand Steering network is shown on sheets 21 and 22. This network is a series of gates that accepts inputs from the AAU Register and signals from the Control Electronics Board to select the operation to be performed by the AAU Adder. The outputs from this network are sent directly to the B-inputs of the AAU Adder.

The AAU Register is shown on sheets 19 and 20. It is composed of three 4-bit bistable latches (type 7475) that are synchronously clocked by signal AARCLK. The complemented outputs ($\overline{Q}$) of the latches are sent directly to the input gates in the AAU Steering network. These signals are identified as AAR00* through AAR11*. The gating network connected to the output of

the latches enables this register to the Memory Data Bus and the Memory Address Bus, when the appropriate control signals are enabled (AAR/MAR and AAR/MDB).

5.2.8 Character Register

The Character Register (CHR) and its steering network are discussed as a unit (see sheets 23 and 24).

The register (sheet 23) is composed of one and one-half 4-bit bistable latches (type 7475) that are synchronously clocked by signal CHRCLK. Both outputs (Q and $\overline{Q}$) of the latches (M59 and M60) are connected to a group of gates that select and drive the outputs to the Arithmetic Bus (ARB) or the Auxiliary Arithmetic Bus (AAB). The selection is made by two enabling signals: OPDG04I which enables 6-bits to the ARB, and CURAAB which enables 6-bits to the AAB. This distinction is made because some operations combine the 6-bits from the Character Register with the 6-bits from the Line Register and consider the 12-bit combination as the Cursor Register. In this case, the steering is done from the Auxiliary Arithmetic Unit Register. The inputs to the register are obtained from the Character Register Steering network. They are identified as CHR00 through CHR05, but via the network logic they are shown to come from the Auxiliary Arithmetic Unit Register or the Accumulator Register.

The steering network is composed of three type 7451 dual 2-wide 2-input and-or-invert gates (see sheet 24). Any given pair of and gates has one gate associated with a bit from the Auxiliary Arithmetic Unit Register (AAR00-05) and the other associated with a bit from the Accumulator Register (ACR 00-05). An enabling signal associated with each register is anded with the appropriate bits. A low AARCUR signal on board connector pin B13 enables 6-bits from the Auxiliary Arithmetic Unit Register to the Character Register. A high OPDG05I signal on board connector pin A34 enables 6-bits from the Accumulator Register to the Character Register.

5.2.9 Line Register

The Line Register (LIR) and its steering network are discussed as a unit (see sheets 25 and 26). The unit is almost identical to the Character Register: the same type logic elements are used and the source and destination of the data are identical. Some signals are different. In the steering network, the inputs from the Auxiliary Arithmetic Unit Register are bits AAR06 through AAR11 and the enabling signals are AARCURB and OPDG03I. In the Line Register, the Arithmetic Bus enabling signal is OPDG02I.

5.2.10 Accumulator Register

The Accumulator Register (ACR) is the primary arithmetic and logical register of the TPU. It is an 8-bit register that contains the data for the output bus and receives data from the input bus. The logic for the ACR is shown in sheets 27 and 28. It consists of eight type 7472 J-K master-slave flip flops, bus drivers and input/output inverters. The ACR is the only register on the Data Flow board that uses J-K flip flops instead of simple latches. The flip flops prevent racing which might occur when an arithmetic operation is performed on the contents of the ACR and then loaded back into it. The input-and gates that are integral with the flip flops allow anding and oring of input data without additional logic gates.

The input to each flip flop is a bit from the Arithmetic Unit Adder. For example, bit ARA00 is sent to flip flop M31 (ACR00). It is connected directly to the J-input and gate but it is inverted by M15 (ARAI00) before going to the K-input and gate. Each flip flop is connected in the same manner. The Or disable signal ACRKIN is connected to each K-input; and the And disable signal ACRJIN is connected to each J-input. The third input of each J and K-input is left unconnected which means that it is always high (1). All flip flops are synchronously clocked by signal STRBACRL from the Control circuit board.

The output of the ACR flip flops goes to the ARU steering circuit, CHR, and LIR steering directly; to the output bus via inverters such as M15 (OTB00) for bit 00; and to the MDB and ARB via drivers such as M 111, M23 and M19. Three enabling signals are provided to transfer the contents of the ACR to these two buses. They are: ACR/ARB which enables ACR bits 00-03 to

ARB bits 04-07; BED11 which enables ACR bits 00-07 to MDR bits 00-07; and BED10 which enables ACR bits 00-07 to MDR bits 08-15. These last two transfers represent the two 8-bit bytes of a memory word.

5.2.11 Condition Store Register

The Condition Store Register (CSR) is a 3-bit register that stores the status of all arithmetic operations. Sheet 29 shows the logic for the register and its associated steering network.

The register consists of a type 7475 4-bit bistable latch M41; however, only 3-bits are used: CSR00 represents Carry-Out and sets on an overflow condition from an AAU or ARU operation; CSR01 represents an Equal condition and sets if the result is zero after an AAU or ARU operation; and CSR02 represents a Negative condition and sets if the MSB of the ARU operation is 1. The Negative condition is not an important consideration because the system deals basically with positive numbers.

Three drivers MDBCS00, 01 and 02 are used to enable the CSR outputs to the MDB and hence to the MDR and memory.

The steering network is a multi input decoding circuit that consists of M57, M73, M89, M125, etc. The gates at the left side of the sheet accept the 12-bits from the Auxiliary Arithmetic Adder and they are anded at M106 (CS021) to decode a Zero condition.

5.2.12 Program Counter Register

The Program Counter Register (PCR) is a 12-bit register that contains the address of the next instruction to be executed. The least significant bit is always zero. The logic for the PCR is shown on sheets 30 and 31.

The PCR is composed of three 4-bit bistable latches (type 7475) that are synchronously clocked by signal PCRCLK. The PCR is incremented by going through the Auxiliary Arithmetic Unit (AAU). The AAU adds 2 to the count and returns this updated count to the PCR. The input to the PCR is the 12-bits from the Auxiliary Arithmetic Register. These bits are identified as AAR01 through AAR11; actually, bit AAR00 is not transferred (bit 00 always = 0). Each latch Q output has an associated driver that is connected to the Auxiliary Arithmetic Bus (AAB). They are identified as M52, M53 and M56.

Three enabling signals are used to effect the transfer from the PCR to the AAB. The signals are: PCR/AAB which enables bits 01-08; PCR/AAB9 which enables bit 9; and PCR/AABM which enables bits 10 and 11.

All data movement depends on knowing whether the program is in the top sector or not. If bits 09, 10 and 11 (2K system) are high, the current sector is the top sector. This is indicated by anding bits PCR09, PCR10 and PCR11 in M1 (TOPSEC), which is enabled when both inputs are high.

5.2.13 Test Comparator

The Test Comparator is a decoding network that tests the outputs of the Condition Store Register, Memory Data Register bits 00, 02, 08, 09 and 13 and Accumulator Register bit 00 to determine which operation to perform. The network is constructed like a multiplexer with the input gates channeling to an enabling gate M109 (TCD20) to the Control board. The Carry-Out signal CSR00 is anded with MDR08 at gate M9 (TCD14). If a Carry-Out is not present (CSR00 is high) and MDR is set (high), the condition is true and M109 is enabled. The Zero condition signal CSR01 is anded with MDR09 at gate M9 (TCD13).

The next gate M74 (TCD12) tests for a Negative condition via signal CSR02. The last gate M74 (TCD11) tests for the Accumulator Register being odd via signal ACR00. Each of the last 2 gates has three other inputs: MDR00, MDR01 and a common input from M90 (TCD30). The inputs to M90 are MDR02 and MDR13.

5.2.14 Bus Enable Decoders for the MDR

The Bus Enable Decoder circuitry generates the signals that enable the bus drivers associated with the Accumulator Register (see paragraph 5.2.10) and the Memory Data Bus (see paragraph 5.2.3). The logic for the Bus Enable Decoder is shown on sheet 33.

Notice that six bus enabling signals are generated by gates M10 and M26. These signals actually enable bus drivers associated with transferring data from the Accumulator Register to the Memory Data Bus and from the Memory Data Register to the Arithmetic Bus. Each signal enables eight bus drivers.

Refer to the left side of the sheet. M10 (BED10) enables ACR00-07 to MDB08-15 and M10 (BED11) enables ACR00-07 to MDB00-07. These gates are enabled by control signal ACR/MDB anded with a byte selection signal from M26 (BED25) or M11 (BED26). Byte selection is necessary because the ACR is an 8-bit register and the MDR is a 16-bit register. The byte selection is determined by the inputs to M26 (BED25) which are MAR00 and OPR04. If the output of M26 (BED25) is low, the gates associated with transferring bits 1 through 7 are enabled: these gates are M10 (BED11), M10 (BED13) and M26 (BED15). If the output of M26 (BED25) is high, its output is inverted by M11 (BED26) and the gates associated with transferring bits 8 through 15 are enabled: these gates are M10 (BED10), M10 (BED12) and M26 (BED14).

M10 (BED12) enables MDR08-15 to ARB00-07 and M10 (BED13) enables MDR00-07 to ARB00-07. These gates are enabled by control signal MDR/ARB I anded with a byte selection signal from M26 (BED25) or M11 (BED26).

M26 (BED14) enables MDR08*-15* to ARB00-07 and M26 (BED15) enables MDR00*-07* to ARB00-07. These gates are enabled by control signal MDR*/ARB anded with a byte selection signal.

5.2.15 Memory Data Register

The Memory Data Register (MDR) is a 16-bit register that buffers all data to and from the memory. The logic for the MDR is shown on sheets 4 and 5.

The register consists of four 4-bit bistable latches (type 7475) that are synchronously clocked by three signals. ODMDRCLK clocks latches MDR00 through MDR07; EVMDRCLK clocks latches MDR08-MDR11; and MDRCLKM clocks latches MDR12 through MDR15. These clock signals allow data to be transferred in bytes. The input to the MDR is the 16-bits from the Memory Data Bus (MDB00-MDB15). The outputs of the MDR go several places; Memory Data Bus Drivers, Test Compare Decoder, Condition Status Register and Exclusive-Or Unit. The Memory Data Bus Driver logic is significant because it enables the MDR to the ARB and AAB. It is discussed in the next paragraph (5.2.16).

5.2.16 Memory Data Bus Drivers

The logic for the Memory Data Bus Drivers is shown on sheets 8 and 9. The Q outputs of the Memory Data Register are connected to 16 Arithmetic Bus Drivers labeled ARBMD00 through ARBMD15 (gates M55, M54, M51 and M50). The Q outputs of the MDR are connected to 16 Arithmetic Bus Drivers labeled ARBMD00* through ARBM15* (gates M71, M70, M67 and M66). The transfers to the ARB are handled in bytes because the ARB is an 8-bit bus. The $\overline{Q}$ outputs are also connected to 12 Auxiliary Arithmetic Bus Drivers labeled AABMD00 through AABMD11 (gates M87, M86 and M83). Only bits 00-11 are used because the AAB is a 12-bit bus.

The MDR-to-ARB transfers are enabled by signals generated in the MDR Bus Enable Decoder (see paragraph 5.2.14). The transfers and enabling signals are listed below.

Enabler	Transfer
BED13	MDR00 -07 to ARB00-07
BED12	MDR08 -15 to ARB00-07
BED15	MDR00*-07* to ARB00-07
BED14	MDR08*-15* to ARB00-07

The MDR-to-AAB transfers are enabled by signals from the Control board. Signal MDR/AAB enables the transfer of MDR00-08 to AAB00-08 and signal MDR/AABM enables the transfer of MDR09-11 to AAB09-11.

5.2.17 Exclusive-Or Unit

The logic for the exclusive-or Unit is shown on sheet 3. It consists of two type 7486 quad 2-input exclusive-or gates and two type 7403 quad 2-input positive nand gates. This yields eight exclusive-or gates and eight nand gates. The output of each exclusive-or gate is connected to one input of each nand gate. The other input of each nand gate is connected to a common control signal OPD26I. The inputs to the exclusive-or gates are bits from the Memory Data Register (MDR) and Accumulator Register (ACR). All 8-bits of the ACR are used (ACR00-ACR07) and the 8 LSB of the MDR are used (MDR00-MDR07). When the control signal is enabled, the MDR and ACR outputs are exclusive-ored and enabled to the Arithmetic Bus.

5.2.18 TPU Register-Clock Drivers

The TPU Register-Clock Driver circuitry accepts signals from the Control board and generates clock signals for all the register. A single clock signal is used for each register with the exception of the MDR which uses three clock signals: M18 (ODMDRCLK) clocks latches MDB00 through MDR07; M18 (EUMDRCLK) clocks latches MDR08 through MDR11; and M1 (MDRCLKM) clocks latches MDR12 through MDR15. The ACR also uses two clock signals: STRBACRL which clocks ACR00-03 and STRBACRM which clocks ACR0-4-07.

5.3 DATA CONTROL ELECTRONICS

5.3.1 General Information

All the data control electronics are contained on one printed circuit board located in slot 13 (see Figure 5-4).

A simplified block diagram of the data control electronics is shown in Figure 5-5. The circuitry performs a multitude of functions. The discussion is divided into 10 basic areas as follows:

1. Instruction Register and Decoder
2. Generic Opcode Decoder
3. Miscellaneous Control
4. State Counter
5. Auxiliary Arithmetic Unit Control
6. Arithmetic Unit Control
7. Real Time Clock Module
8. Interrupt Controls
9. Controller Decoder and Wired Option Matrix
10. Control Drivers

The discussions are referenced to detailed logic diagram 005-07-01 (16 sheets).

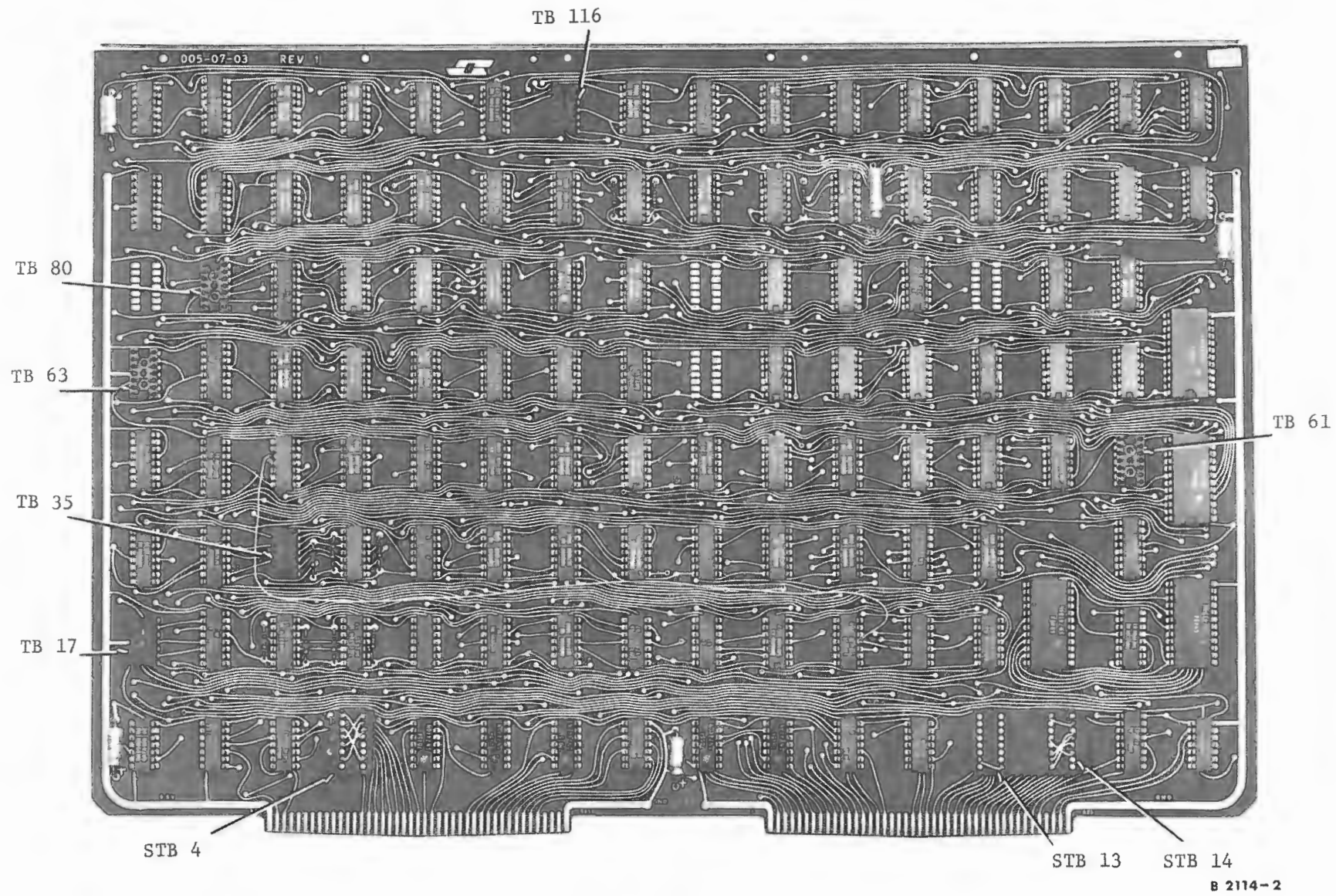


Figure 5-4. Data Control Circuit Module

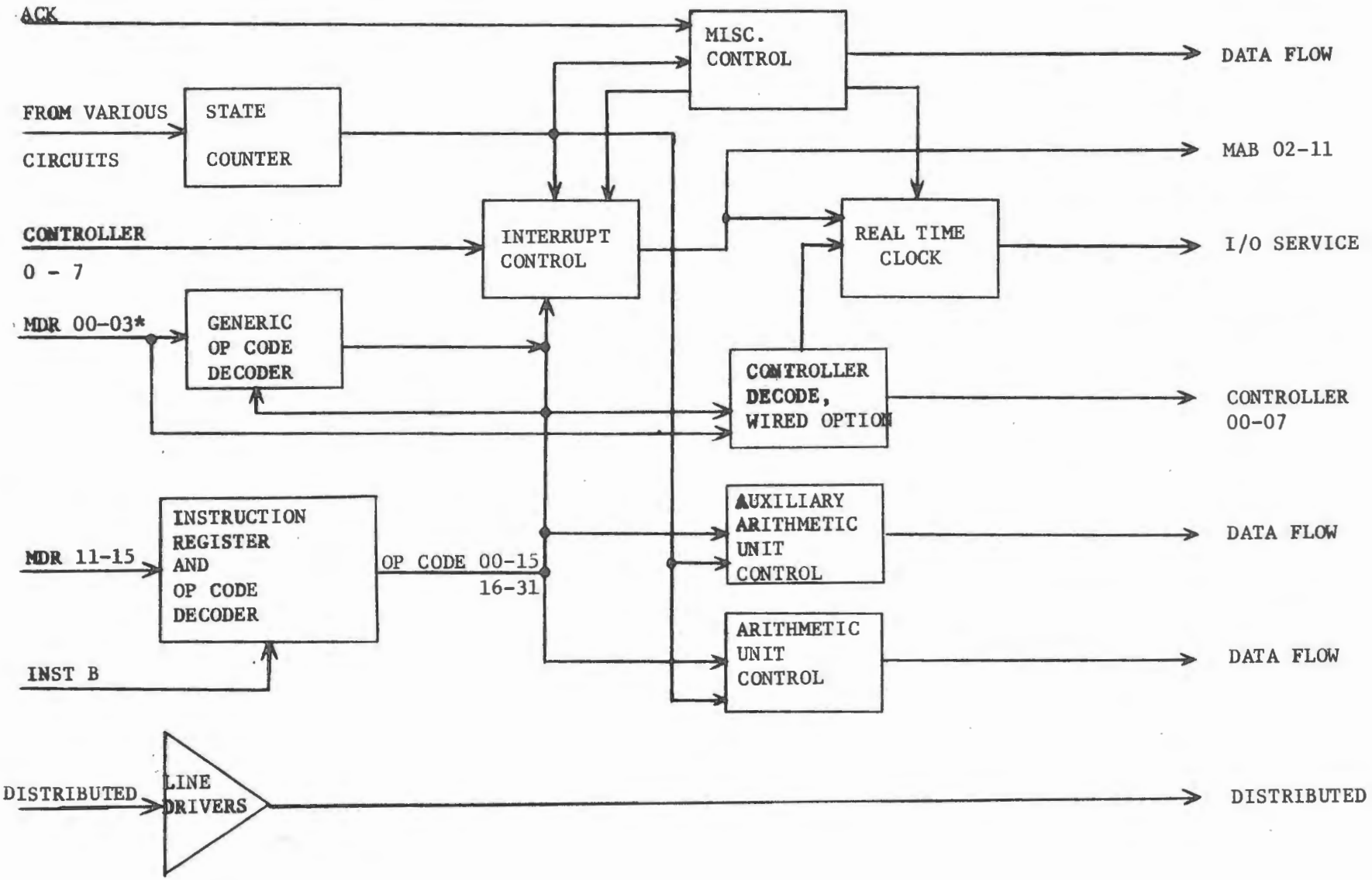


Figure 5-5. Simplified Block Diagram Data Control

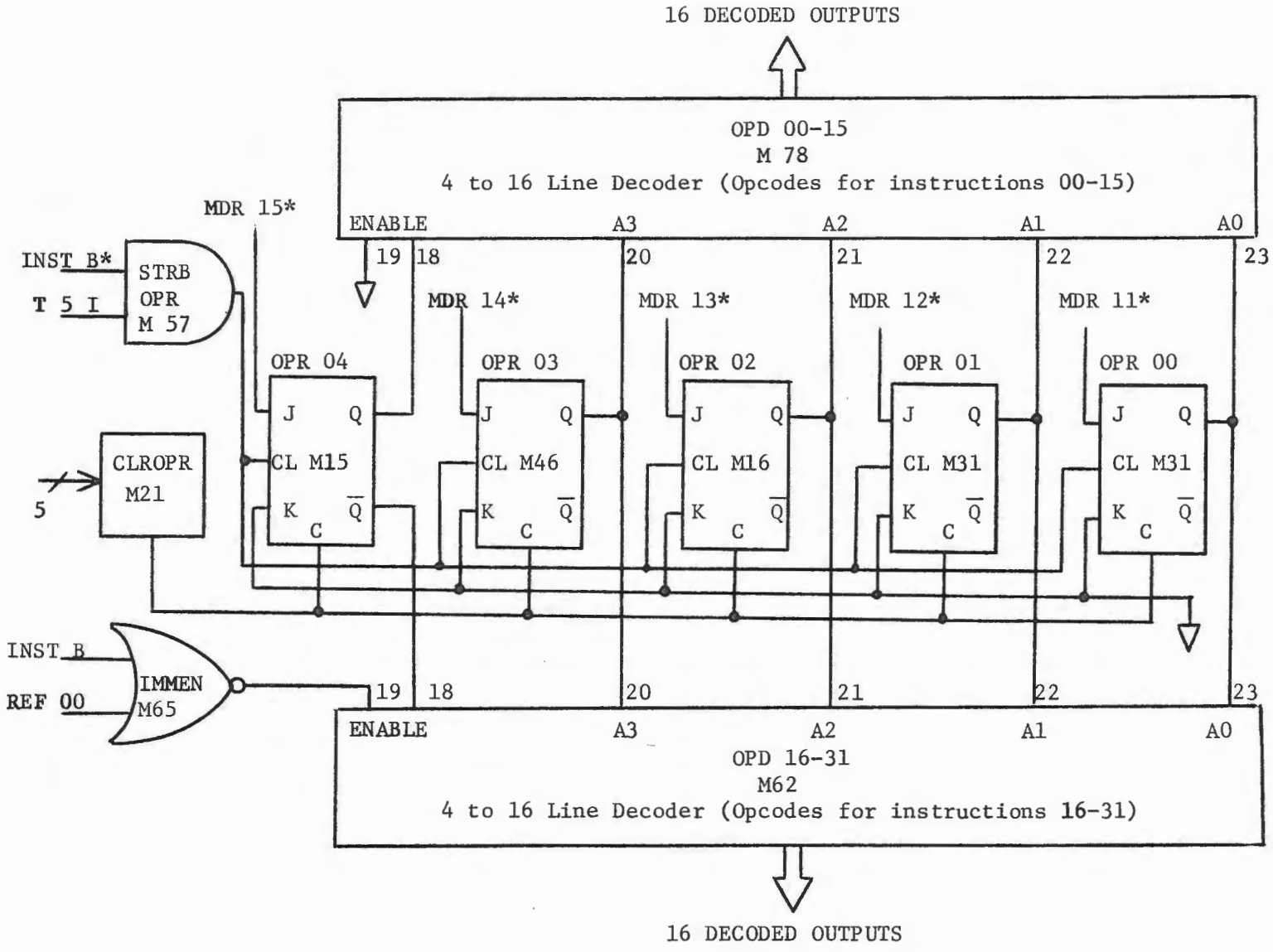


Figure 5-6. Detailed Block Diagram of Instruction Register and Decoder

5.3.2 Instruction Register and Decoder

During the instruction cycle of system operation, the Operation Code (Opcode) portion of an instruction (bits 11 through 15) is obtained from the Memory Data Register (MDR), temporarily stored in the instruction register as a 4-bit binary word and decoded as a unique 16-bit binary word. The decoder output is used during the execute cycle of system operation. Figure 5-6 is a detailed block diagram of the Instruction Register and Decoder. Refer to logic diagram 005-07-01, sheets 2 and 3 for details.

The Instruction Register consists of five J-K master-slave flip flops identified as OPR00 through OPR04. The flip flops are dual IC packages: both units in M31 and M46 are used, while only one unit in M15 is used. The signal to the J-input of each flip flop is an inverted bit from the Memory Data Register. As shown in Figure 5-6, these bits are identified as MDR11* through MDR15*. The K-input of each flip flop is connected to ground, which holds it low (logic 0). The flip flops are synchronously clocked (set) by the output of and gate M57 (STRBOPR). The register is cleared by a low output (logic 0) from M21 (CLROPR). A low input to the CLEAR terminal of the flip flop sets the Q output to logical 0. M21 is a 2-2-2-3 input and-or-invert gate. Refer to sheet 2 for input signal identification and connections. The Instruction Register is used so that the Terminal Processing Unit always knows the instruction that is currently being processed.

Two decoders are used: M78 (OPD00-15) and M62 (OPD16-31). Each decoder is a Texas Instruments type 74154 4-line-to-16-line decoder. Decoder M78 decodes the Opcodes for TPU instructions 00 through 15; M62 decodes the Opcodes for TPU instructions 16 through 31. The decoder is enabled by simultaneous low inputs to pins 18 and 19. Decoder M78 has pin 19 connected to ground (low) and pin 18 connected to the Q output of the Instruction Register flip flop M15 (OPR04). M78 is enabled when the Q output of OPR04 is low, which occurs when the J-input of OPR04 is low. This input is bit 15 of the MDR; therefore, M78 decodes Opcodes that have a 0 in the most significant bit position. Decoder M62 has pin 19 connected to the output of M65 (IMMEN) and pin 18 connected to the complemented output (Q*) of flip flop OPR04. M65 is a 2-input nor gate which produces a low output when either or both input signals INSTB and REF00 are high. Pin 18 goes low when the Q* output of OPR04 is low, which occurs when the J-input of OPR04 is high.

M62 decodes Opcodes that have a 1 in the most significant bit position. When both ENABLE inputs (pins 18 and 19) of the decoder are low, the input data (A_0, A_1, A_2, and A_3) is decoded into one of 16 mutually exclusive outputs. If either ENABLE input is high, all outputs are high and the 4-bit input data word is irrelevant.

In operation, the Memory Data Register is strobed from memory at time T4 of the instruction cycle. Data is available in the MDR concurrent with the leading edge of T4. By time T5, the data is available at the Instruction Register input. On the trailing edge of T5, the Instruction Register is set which presents the data to the appropriate decoder input. The data is decoded during the remainder of the instruction cycle and is available at the decoder output for use during the execute cycle which follows immediately.

The following example shows how the Instruction Register functions to keep the TPU informed about the current instruction being processed. Consider a Store Instruction that stores the contents of the Accumulator in the byte at the effective address. The instruction is decoded during the instruction cycle and the MAR is set to the address where the byte is to be stored. The data is stored during the execute cycle. During the execute cycle, the instruction register holds the 5 bit Opcode of the store instruction. At the end of the execute cycle the PCR and MAR are set to the address of the next instruction. The new instruction is decoded when the instruction cycle is entered. The above process is repeated for the next instruction.

5.3.3 Generic Opcode Decoder

Decoder M32 (OPDG00-15) is used to decode Generic Instructions. Reference detailed logic diagram 005-07-01, sheet 4. It is identical to the decoders used in the Instruction Register and Decoder circuitry (TI type SN 74154). The ENABLE inputs of decoder M32 are connected as follows: pin 19 to ground and pin 18 to output OPD24 (pin 9) of decoder M62 (OPD16-31). This means that M32 is enabled when output OPD24 of M62 is low. In effect during a Generic Instruction. The truth table for the SN 74154 Decoder (Reference TI Catalog) shows that OPD24 is low for only one specific configuration of the 4-bit input data word as shown below.

M62 Input Pin	20	21	22	23
Logic Level	1	0	0	0

The inputs to M62 are derived from the Q outputs of the Instruction Register flip flops OPR03, OPR02, OPR01 and OPR00 which correspond to Memory Data Register bits MDR14*, MDR13*, MDR12* and MDR11*. But MDR15* must be high (logic 1) in order to enable decoder M62. These five bits represent the Opcode portion of the instruction word; and, in this case, the code is 11000 which is the basic code for the class of Generic Instructions. Memory Data Register bits MDR00* through MDR03* are sent to the input of Generic Decoder M32 (OPDG00-15) to identify the specific Generic Instruction.

The presence of a Generic Instruction is actually decoded by M62 which enables M32. The specific Generic Instruction is decoded by M32.

5.3.4 Miscellaneous Control Functions

A multitude of miscellaneous control functions are performed by this board. Refer to detailed logic diagram 005-07-01, sheets 5 and 6. The basic functions are discussed. Because of the complexity of the logic, detailed signal tracing is not performed.

1. Data Transfer from the Auxiliary Arithmetic Register (AAR) to the Program Counter Register (PCR)

Refer to the left side of sheet 5 for the logic involved in a transfer of data from the AAR to the PCR. A high output signal from M73 (AARPCR) indicates that the data transfer is complete. On the Data Flow board, the PCR is always tied to the AAR. When the PCR is clocked, data is transferred from the AAR to the PCR. Data transfer is desired at the end of the instruction, at which time the program desires to proceed to the next instruction. Signal AAR/PCR from M73 is the enabling pulse and indicates that the instruction is complete and data can be transferred. The multiple inputs to M73 indicate that there are several ways of completing an instruction. Note the inputs to M89 (PCCA12). If the state counter is in the INSTB state and the Opcode is greater than 16 and not a jump indirect, not a successful test and

is not an I/O acknowledged, then all activity is complete. M89 is enabled which in turn enables the AAR/PCR signal.

2. Program Counter Register Strobe

The output of M73 (AARPCR) is also an input to M58 (STRBPCR) which produces a clock signal that is used to strobe the PCR. Another input to M58 is REGRST which is present when the PCR is to be reset. An Instruction Complete signal (AARPCR) and a PCR reset signal (REGRST) both enable a PCR strobe signal. When strobe PCR is enabled the strobe occurs at time T19.

3. Memory Address Register Strobe

The Memory Address Register (MAR) is always strobed at time T19. The strobe signal STRBMAR is generated by M53 (T19INH). The inputs to M53 are the inverted clock pulse at T19 (TIME 19I) and the WAIT signal. The Wait state indicates an idle condition during which the TPU is waiting for an interrupt. During this period, the MAR is not strobed. The WAIT signal is high during this idle condition and the inverted T19 pulse is always low when it is present. An incoming TIME 19I pulse enables M53 only when the WAIT signal is low (no idle condition).

4. Data Transfer from the Arithmetic Unit (ARU) to the Accumulator Register (ACR)

An enabling signal is required to control the transfer of data from the ARU to the ACR. The enabling signal ARU/ACR is generated in M73 (ARUACR). The output of M73 is inverted by M104 to produce the ACR strobe signal (STRBACRL). The multiple inputs to M73 indicate that several conditions can control the transfer of data. One input is the Boot Wait (BTWAIT) signal to input pin 9 of M73. Two of the states involved in the boot sequence require data to be transferred from the ARU to the ACR. The BTWAIT signal is used as the enabler in this case. Several inputs to M74 are used as enablers. Some are: the Read I/O and Acknowledge signal RIOACK (pin 9) controls reading in I/O data; the Subtract Immediate signal OPD19 (pin 13) is a one-cycle

instruction that contains data in the instruction word; and the Boot Shift signal ACR/ARBI (pin 10) that indicates the four least significant bits of the boot input data are to be transferred.

5. Line Register Strobe

The Line Register (LIR) contains the six most significant bits of the Cursor Register (CHR); it represents the number of the line on which the cursor is displayed. M11 (STRBLIR) generates a strobe to enable the LIR. One of the cases when a Line Register strobe is required is when the Move Accumulator to Line signal OPDG03 is low at pin 1 of M76 (LIC10), output pin 6 of M76 goes high. This signal goes to pin 1 of M11 (STRBLIR) and when a high T14 clock pulse arrives at pin 2, the strobe is generated at pin 3. The LIR strobe is low when enabled. The strobe goes to the Line Register logic on the Data Flow board.

6. Data Transfer from the Auxiliary Arithmetic Unit (AAU) to the Character Register (CHR) and the Line Register (LIR)

System operation requires data to be transferred from the AAU to the CHR and LIR. (Together, the CHR and LIR form the Cursor Register.) An example is loading of the data that defines the cursor position in the Cursor Register: the six most significant bits are loaded in the LIR and the six least significant bits are loaded in the CHR. The data is obtained from the AAU and the transfer requires an enable signal and two strobes. The enable signal is generated by M60 (AARCUR) and is low when enabled. The gating that steers M60 combines EXEC B with an appropriate signal during the execute cycle of system operation. M60 (AARCUR) is enabled when both its inputs (pins 9 and 10) are high. Pin 9 is connected to EXEC B, so it is high when EXEC B is high. The state of pin 10 is determined by three other signals. The Cursor Addressed signal MARCUR and CSC20 must both be high. This produces a low input to pin 13 of M60 (CUC10). The other input of this gate (pin 12) is connected to the Load Cursor signal OPD08 which must be low. These low inputs (pins 12 or 13) to M60 (CUC10) produce a high output to pin 10 of M60 (AARCUR). During the EXEC B state both inputs (pins 9 and 10) of M60 (AARCUR) are high and the enable signal is generated.

The enable signal is also sent to M76 (LIC10) and M76 (CHC10) which are inputs to strobe generators M11 (STRBLIR) and M11 (STRBCHR), respectively. The logic that gates the transfer by producing the AARCUR enable signal also defines strobing of the LIR and CHR. The strobe is generated only when a high T14 clock pulse is also present at the input of M11 (pin 2 for STRBLIR and pin 4 for STRBCHR).

Other paths are available to define strobing of the LIR and CHR. A Register Reset signal REGRSTI generates both LIR and CHR strobes. A Clear Line Register signal OPD612 or a Move Accumulator to Line signal OPD603 generates a LIR strobe. A Clear Character Register signal OPD613 or a Move Accumulator to Cursor signal OPD605 generates a CHR strobe. In each case, the input signal must be low to generate the strobe.

7. Memory Data Register Strobe

System operation provides strobing of the memory at time T4. The strobe signal is generated by M56 (MEMSTRB) and inverted by M104 (MCMSTRBI). M56 is one section of a triple 3-input positive nand gate. The three inputs are time pulse T4, WAIT*, and INSERT. In normal operation, the system is not in either the Wait or Test state and both WAIT* and INSERT are high. Under these conditions, M56 is enabled each time a high T4 pulse is applied to pin 13. The enabled output of M56 is low and is inverted in M104 (MCMSTRBI) to provide a high Memory Data Register strobe (STRBMDR). The strobe reads the data on the MDB into the MDR.

During the Wait state, which is an idle period, the MDR strobe is inhibited by a low WAIT* signal.

During the Test mode, the TPU is connected to the test console. The INSERT signal is controlled from the console and allows data to be inserted into the memory from the console during testing. When the INSERT signal is low, the MDR strobe is inhibited. This allows data to be loaded into the MDR and subsequently stored in memory via the individual pushbuttons on the test console

8. Transfer of Data from the Accumulator Register to the Memory Data Register

An enable signal is required to transfer data from the Accumulator Register (ACR) to the Memory Data Register (MDR). The signal is ACR/MDR and it is generated by M27 (ACRMDB); it is low in the enabled state. The associated gating (M43 and M29) shows several paths for enabling the ACR/MDR signal. The gating signals are channeled eventually to pin 1 of M27 and a timing signal from M27 (BYPASS) is applied to pin 2. Both inputs must be high in order to enabled M27 (ACRMDB). An enabling path to M27 pin 1 is completed if a Store instruction (OPD01I) is present and the system is in EXEC A. These signals are applied to M43 (MDCC20) and both must be high. Another enabling path is completed at the end of each BOOT character transfer and is sensed by signal BOOTX going low.

Once the data transfer is enabled to the MDR, a strobe is required to read it in. The strobe signal is generated by M12 (STRBBYTE). It is a byte strobe because the ACR contains only 8-bits and reads in only half a memory word. One input to M12 (STRBBYTE) is the ACR/MDR signal from M27. The other input is a low T9 pulse. When both inputs are low, a high STROBE MDR BYTE signal is generated. The strobe is timed to occur at T9 to allow transfer of the data to the memory during the memory restoration cycle.

9. Transfer of Data from the Auxiliary Arithmetic Unit to the Memory Data Register

The instructions that control this data transfer are concerned with operations that require 12-bits of data to be read into memory. An enable signal is required to transfer the data from the Auxiliary Arithmetic Unit (AAU) to the Memory Data Register (MDR) from which it is subsequently read into the memory. The signal is AAR/MDR and it is generated by M11 (AARMDB); it is low in the enabled state. The associated gating (M90, M43 and M27) shows several paths for enabling the AAR/MDR signal. The gating signals are channeled eventually to pin 12 of M11 and a timing signal from M27 (BYPASS) is applied to pin 13. Both inputs must be high in order to enable M11 (AARMDB). An enabling path is completed if a low Store Cursor signal OPD09 is present and the system is in EXEC A.

10. Memory Data Register Strobe for Bits 00 through 11

Certain instructions exist in which it is undesirable to strobe MDR bits 12 through 15. An example is the Increment instruction in which the data in the AAU is taken and a 12-bit transfer is performed; therefore, separate strobe signals are generated for bits 00-11 and bits 12-15. The strobe signal MDR 00-11 is generated by M12 (STRBMDR). It is generated by either a high MEMSTRBI signal or a low T9I pulse and a low CLKMDRI signal at the inputs of M12 (MDCA60).

10a. Accumulator J/K Enable Gates

M122 and M123 provide the signals for enabling the and-function and the or-function performed in the Accumulator Register on the Data Flow board. (The following items (11-16) are referenced to 005-07-01, sheet 6.)

11. Circuit for Enabling Special Addressing of the Memory Address Bus

Normally, the Memory Address Bus (MAB) is enabled from the Auxiliary Arithmetic Unit. Special addressing uses another path that allows a direct load into the MAB, which occurs specifically during the Auto Exec routine and during power restart. Refer to the SPD 10/20 Programmers' Reference Manual for details of the Auto Exec routine.

Gating of the special address to the MAB is required at three times during the Auto Exec routine; i.e., when entering Auto Exec as a result of an interrupt, during the Ext D state and when entering Auto Exec because of an unacknowledged RIO or WIO. Gate M70 (MACA10) is used in the first case. On completing each instruction AAR PCR is high, and if the state counter is not in Ext Z and if there is an interrupt, then all inputs to this gate are high, generating an enable signal to M118 SPAMAB. For this case of entering Auto Exec on a controller interrupt, the address that will be gated on the MAB is the Interrupted Program Save Address (FF8). At FF8 the ACR and CSR for the interrupted program will be saved. The next address required on the MAB is FFA for saving the PCR. This address is not obtained via the special address but instead is handled by transferring the address in the MAR (FF8) to the AAB and in turn adding +2 to the address, with the result FFA being

transferred back to the MAR. At FFA the PCR for the Interrupted Program is saved. At this point the state counter enters state "Ext D" (Case 2) and the save address for the interrupting controller must be gated to the MAB. This is achieved by bringing a low signal to Pin 9 of M118. Assuming the interrupting controller was device 2, the low on Pin 9 would result in FE8 being gated to the bus. (Data for the ACR and CSR would be fetched from this address. Data for the PCR return would be fetched from address FEA by performing a T2 operation in the AAU.) When entering Auto Exec because of an unacknowledged RIO or WIO (Case 3) gating of the special address to the MAB is required to save the ACR and CSR for the controller. Under these conditions M25 (IONACK) will have all high inputs, and its output will produce a low signal on M118 Pin 13. For the example this will generate address FE8 on the bus and the ACR and CSR will be stored at this address. Again the next address will be achieved by performing a T2 operation in the AAU. Finally, during the "Ext D" state (Case 2) address FF8 is required which again requires negating of the special address to the MAB via a low signal on M118 Pin 9.

The SPAMAB gate is also enabled during a power restart by a low signal on M118-10. This is required to force the MAR to address FFC during power restart.

12. Accumulator Register Strobe

Two signals are used to strobe the 8-bit Accumulator Register (ACR). The strobe for bits 0 through 3 is generated by M86 (STRBACRL) and the strobe for bits 4 through 7 is generated by M86 (STRBACRM). When enabled, both signals are high. Two strobes are used because of certain conditions encountered during Boot operation. Both strobes are timed at T17, but different enablers are used. If the ARU is enabled to the ACR (signal ARUACRI) and T17I is present, bits 0 through 3 are strobed. The strobe appears at pin 13 of M86 and is identified as ACR 0-3. Bits 4 through 7 are also strobed but another enabling signal is used because of the boot signal BOOTWAITB at pin 9 of M117 (ACCS12). In Boot operation, bits 4 through 7 are the most significant bits. During Boot transfers 8-bits are loaded to the ACR, then shifted left (loosing 4), then during BOOTWAITB an additional 4-bits are entered in position 0-3. Bits 4 through 7 (MSB) must not be strobed during BOOTWAITB.

The following conditions are required to enable the strobe for bits 4 through 7: ARU enabled to ACR (M117, pin 10); system not in BOOTWAITB (M117, pin 9); and TIME 17I pulse to M86, pin 9.

13. INDXB Flip Flop

M118 (INDXB) and M119 (INDXB*) are connected as a RS flip flop which is a simple latch. The set(s) input is SUCC TEST, PWR RST or Jump indirect; and the reset (R) input is INSTA to M119, pin 13. This flip flop is used to insure correct operation of JMP IND, TI/O, CJXX and JCXX instructions and during PWR RST.

14. I/O Acknowledge Signals

Two signals are provided to indicate whether or not an I/O has been acknowledged. The Read I/O Acknowledged signal is generated by M26 (RIOACK) and the Read I/O Not Acknowledged signal is generated by M25 (IONACK). Both signals are low when enabled. The inputs that are required to enable the signals are shown on the logic diagram (sheet 6, center section). M101 (ACKI) accepts a low Acknowledge signal from the I/O bus and inverts it to provide an I/O ACK signal. This signal is inverted again by M101 (ACKII) to produce an I/O Not Acknowledged signal (I/O NACK).

M101 (BOOT I) and M101 (BOOT II) produce signals to indicate whether or not the system is in Boot.

15. Register Reset Signals

Signals for reseting registers are generated in three ways via M117, M101 and M85 (reference right side of sheet 6). A low RESET I/O signal to pin 5 of M117 (IORST) provides a high output to inverter M85 (RESET) which produces the low reset signal to the I/O bus.

Either of two input signals to M117 (REGRST) produces three reset signals to clear all registers. The signals are ENTRY, which indicates entry into Boot; and the power reset signal PWR RESET. When either of these signals is low, a high REG RESET signal is generated at pin 11 of M117 (REGRST). This signal is inverted by M101 (REGRSTI) to provide a low REG RESET signal. This signal is sent to M117 (IORST) and then to M85 (RESET) to produce a low RESET to I/O BUS signal.

When the terminal is connected to a Test Console, pin 12 of M117 (REGRST) is connected to a switch that resets the system.

16. Memory Address Register Strobe

The output of M37 (STRBMAR) is the strobe signal for the MAR. The strobe is enabled when it is low. M37 is an and-or-invert gate with 4-dual input and gates. A high output at any and-gate enables the strobe. When the Refresh Signal REF01 is present at pin 9 and a TI/O pulse is received at pin 10, the MAR is strobed. When the REGRST signal is present at pin 1 and a T17 pulse is received at pin 13, the MAR is cleared. Also on every T19, pin 3 is high producing an MAR strobe. Unused inputs are connected to ground.

5.3.5 State Counter

The State Counter Logic is contained in Logic diagram 005-07-01, sheets 7, 8 and 9. The following items (1 and 2) are referenced to sheet 8.

1. Extension Flip Flops

The first four flip flops on the left side of sheet 8 are the Extension flip flops that determine the four states of the Auto Exec routine. Each flip flop and its control function is listed below.

M33 (EXTW) - Stores data that is in the Accumulator Register and the Condition Status Register

M33 (EXTX) - Stores data that is in the Program Counter Register

M47 (EXTY) - Fetches data for the Accumulator Register and the Condition Status Register

M47 (EXTZ) - Fetches data for the Program Counter Register

The gating shown above the flip flops decodes the states and generates the control signals. The flip flops are synchronously clocked by pulse T20. They can be simultaneously cleared by a low State Counter Reset signal SCRRSTB1. The J-input of M33 (EXTW) is conditioned by the output of M23 (XTCIO). The J-input of each succeeding flip flop is conditioned by the Q-output of the preceding one.

2. Boot State Flip Flops

The last three flip flops determine the states of the Boot cycle. The flip flops are synchronously clocked by pulse T20. They are conditioned by gates M67 (BTC24), M67 (BTC14), M39 (BTC12) and M38 (BTC10). The flip flops are M18 (BOOT00), M18 (BOOT01) and M34 (BOOT02). They can be simultaneously cleared by a low BOOTCLR signal. The following operating sequence is discussed without reference to detailed signal flow. The counter states, which are control signals, are listed below.

000	Not in BOOT
001	ENTRY
010	8 BITS
011	SHIFT
100	4 BITS
101	LOAD MDR

The counter is cleared (000) to prepare for Boot entry. State 1 (001) activates the Boot ENTRY state. State 2 (010) occurs when the Acknowledge signal is received and 8 bits of data are brought in. State 3 (011) performs a shift operation during which the four least significant bits of data are transferred to the four most significant bits of the Accumulator Register. State 4 (100) loads four bits of data into the four least significant bits of the Accumulator Register. State 5 (101) loads the eight bits into the Memory Data Register and is followed by a return to the Wait state for the next character. The gating shown above the flip flops decodes the states and generates the control signals. When the Boot cycle is complete, the Boot line is used to enable the Program Counter Register and start execution of the instruction. M53 (BTC60) controls this function. As long as the high I/O BOOT signal is present at the input of pin 8 on M53, a Boot Inhibit signal is produced. When the I/O BOOT signal is low, the Boot state counter goes to the Wait state at which time the counter is cleared and the Program Counter Register is enabled to the Auxiliary Arithmetic Bus (AAB). A zero is added to the AAB and it is loaded back into the PCR; execution now starts on instruction zero.

The following items (3 through 5) are referenced to 005-07-01, sheet 9.

3. Indirect Flip Flop

The Indirect state of operation is specified when flip flop M81 (IND00) is set. The J-input of M81 is conditioned by M54 (NDC22) and M69 (NDC12); its K-input is conditioned by M15 (INDCUR) and M45 (NDC20). M81 is clocked by pulse T20 and it is cleared by a low SCRRSTB1 signal. If bit 10 of the instruction word is high, the Indirect state is set. Bit 15 of the address word is tested and if it is set, the operation is still in the Indirect state. The loop continues until an address is found in which bit 15 is not set. This is the address of the next instruction to be executed. The state of MDR15 to pin 1 of M45 (NDC20) is used to clear out of Indirect operation.

4. Wait Flip Flop

Flip flop M81 (WAIT) is set during the Wait state. It is conditioned by M38 (WAITEN) and is clocked by pulse T17. Its outputs are sent to the Memory Address Register Strobe circuitry on sheet 5. Reference paragraph 5.3.4, item 3, which discusses the Wait state.

5. Refresh Flip Flops

Flip flops M95 (REF00) and M95 (REF01) are used to establish the Refresh cycle control signals. The flip flop inputs are conditioned by M114 (RFC16), M114 (RFC14), M98 (RFC12) and M98 (RFC10). They are clocked by M83 (REFCLK) and cleared by a low SCRRSTB1 signal. The gating shown above the flip flops decodes the states and generates the control signals.

The following items (6-9) are referenced to 005-07-01, sheet 7.

6. Power-Up Cycle

During the Power-Up cycle, the computer is being activated and all previous states must be cleared to insure that operation starts at the correct point. Refer to the left side of sheet 7 for the Power Up cycle circuitry.

When the +5 volts is first applied the RC network R3 and C1 produces a low level on M34 pin 7 setting the Power Up flip flop (Q = 1). After a period of time (determined by R3 and C1) the preset input to M34 (pin 7) is high. M34 is set to the Power Up state; Q = 1 and the preset input is disabled. The

low signal from the $\overline{Q}$ output of M34 causes a high signal from M100 (SCRRST) to pin 5 of M85 (SCRRSTB1). Pin 4 of M85 is connected to a free running clock. When a high clock pulse appears, M85 is enabled and a low signal is produced that clears eight flip flops in the State Counter. Also a low is applied to M99 pin 5 which produces, upon entering the Boot state, a high output to M99 pin 1 which in turn is anded with two other signals to clear the three Boot flops. The ENTRY signal is high (pin 13 of M100). This signal is also sent to pin 4 of M99 (BOOTCLR) where it is anded with the PWR UP signal. Thus when the TPU is in BOOT entry $\overline{\text{PWRUP}}$ M99-6 is low producing a low on M100 pin 3 which clears all the non Boot state flip flops. When the Refresh and Timing board has gone through the Power Up cycle, system clock signals are generated. The first T20 pulse, which is the clock input to M34, clears out the Power Up cycle.

7. Power Reset Cycle and INSTB Flip Flop

The Power Reset cycle is used to enable the special address to the MAR which contains the instruction that starts the particular program. Flip flop M48 (PWRST) has been conditioned by M34, so when the first T20 pulse arrives, M48 is set and produces a low signal at its $\overline{Q}$ output. This is the power reset signal PWR RESET. Flip flop M48 (INSTB) is conditioned by M51 (NSCIO) so that T20 pulse sets it to provide the INSTB signal. This flip flop sets and resets during the instruction cycle of system operation. A low PWR RESET signal to pin 10 of M40 (EXC12) conditions the EXEC flip flop M64 so that the next T20 pulse sets M64 which initiates the execute cycle of system operation. Briefly, the operating sequence is as follows: after going through the Power Up state the Power Reset state occurs and the Power Restart Address (FFC) is loaded into the MAR. The next state is the Execute state. During this state the contents of the MDR (Bit 00-11) at FFC are loaded into the MAR and PCR and program execution is started. This sequence starts the program running again after a power down has occurred.

8. Execute Cycle

During the execute cycle, the system executes non-immediate class instructions. Flip flop M64 (EXEC) is set during the execute cycle. Flip flop M64 (EXECX) is used only during a Cursor Compare instruction, which is the

only three cycle instruction. M64 (EXEC) is conditioned by M40 (EXC12) and M24 (EXC20). M40 (EXC22) provides channels inputs to M40 (EXC12). The Execute A and Execute B signals which split the execute cycle into two halves, are generated by M86 (EXECA) and M86 (EXECB), respectively. Both these signals are high when enabled. When M64 (EXEC) is set, it provides a low input to both M86 gates. The other low signal is provided by the Timing Unit Register time 4. TURT41* is connected to M86 (EXECA) and is low during the first half cycle; TURT4I is connected to M86 (EXECB) and is low during the last half cycle.

When the Terminal is connected to the Test Console, signals can be monitored and displayed on lights to indicate the state of operation. For example, TB80 - 14 indicates the state of the EXECX flip flop.

9. State Counter Gating

The cycling of the State Counter is controlled by M70 and M54 (right side of sheet 7). For example, the output of M70 (EXC60) is the signal that starts the Instruction B cycle. When enabled, this signal is low so that the three inputs to M70 (EXC60) must be high. To enable the gate, the input conditions are: presence of a completion pulse AARPCR; no interrupt present; and not in Refresh state.

5.3.6 Auxiliary Arithmetic Unit Control

The logic that controls the Auxiliary Arithmetic Unit (AAU) is shown on sheets 10 and 11.

Refer to the left side of sheet 10. When enabled, M43 (LOW/AAB) forces bits 9 through 11 low (Logic 1) on the Auxiliary Arithmetic Bus. These are the three most significant bits of a 12-bit address. The functional division of a 2K memory and the format of a one-word memory reference instruction are discussed and illustrated in paragraph 4.3.5. To address the top sector, bits 9 through 11 must be a logical (1) as controlled by M43 (LOW/AAB).

M123 (MDRAABM) controls the transfer of bits 9 through 11 from the Memory Data Register (MDR) to the Auxiliary Arithmetic Bus (AAB). There

are several paths to enable this transfer. Both inputs to M123 (MDRAABM) must be high to enable the transfer. One input (pin 9) comes from M123 (AACM10); the other input comes from M106 (MDRAAB) which transfers bits 0 through 8 from the MDR to the AAB when it is enabled. The transfer is performed during the INSTB state if there is a Jump. The enabler is an INSTB signal anded with a Jump Instruction (OPD23) in M123 (AACM10). If the cursor is not addressed and the system is operating in the Indirect state, a transfer is effected. The conditions are a high Cursor Addressed signal MARCUR to M105 (MARCURI) and a high Indirect B signal to M122 (AACM28). The INDXB signal to M122 (AACM18) also enables a transfer. This signal is generated by the latch circuit on sheet 6 that is set by a Jump Indirect instruction or a Power Reset signal or a successful test.

The Program Counter Register (PCR) is enabled to the Auxiliary Arithmetic Bus (AAB) by M44, M45 and M59. In an addressing operation, identifying the current sector in the memory requires examination of PCR bits 9, 10 and 11. The bits are examined and identified by transferring them from the PCR to the AAR. Refer to paragraph 4.3.5 for a discussion of an Effective Address Calculation. M59 (PCR/AABM) enables the transfer of bits 10 and 11; M45 (PCR/AAB9) enables the transfer of bit 9. M44 (PCR/AAB) enables the transfer of bits 0 through 8 from the PCR to the AAR. There are several paths that enable this transfer. The associated gating is channeled to M44 (PCR/AAB) where a high output enables the control signal to transfer the bits. The associated gating is M74 (AACP10), M90 (AACP12), M122 (AACP14), M121 (AACP20), M93 (AACP30) and M100 (AACP22). One condition that enables the transfer is the Exec Cycle, which eliminates the Immediate class of instructions. Another enabling condition occurs when the system is in the Instruction B cycle and no I/O Acknowledge is present. These signals (INSTB and IONACK) are inputs to M90 (AACP12). A Jump to Subroutine signal OPDI15 to pin 12 of M122 (AACP14) or an Extension C signal to pin 5 of M44 (PCR/AAB) also effect the transfer of bits 0 through 8.

M10 (CURAAB) produces a control signal that enables the Line Register (LIR) and Character Register (CHR) to the Auxiliary Arithmetic Unit. For example, it is enabled during a Store Cursor Instruction. Associated gating M58 (AACC10), M90 (AACC16), M121 (AACC12) and M124 (AACM22)

are used to insure the proper sequence of operations leading to a transfer of data from the LIR and CHR to the AAU. For example, M121 (AACC12) operates for a Compare Cursor instruction to insure that a comparison is made prior to the generation of the transfer control signal.

M115 (MARAAB) produces a control signal that enables the Memory Address Register (MAR) to the Auxiliary Arithmetic Bus (AAB). There are several paths that initiate the MAR-to-AAU control signal. The associated gating is M98 (BOOTINH) and M121 (AACM30). A low Boot Entry signal BOOT00* to pin 1 of M115 (MARAAB) enables the MAR to AAB control signal. M98 (BOOTINH) is used as an enabler if the Boot cycle is not inhibited. A Jump to Subroutine signal OPDI15 to pin 10 of M121 (AACM30) or an Extension F signal to pin 3 of M115 (MARAAB) also effect the enabling of the MAR-to-AAU control signal. When the Terminal is connected to the Test Console, two additional enabling signals are effective. The DISPLAY signal to pin 5 of M115 allows the data in a particular memory address to be displayed on the Test Console panel. The INSERT signal to pin 4 of M115 allows inserting data in any memory address.

The following discussion is referenced to sheet 11.

M120 (+2AAU) generates a control signal that initiates the+ 2 Operation in the Auxiliary Arithmetic Unit (AAU). The control signal is low, when it is enabled. Several conditions can enable this signal. The associated logic consists of three M103 gates, two M119 gates and one M121 gate. The first gate, M119 (AAC231), is used as the enabler only when the Terminal is connected to the Display Console. A low DISPLAY signal or a low INSERT signal enables the control signal via a high input to pin 5 of M120. During the Display or Insert conditions, the+2 AAU signal is enabled to the AAU which takes the data on the AAB and adds +2 to it. In this case, the +2 Operation is required to obtain a complete memory word (two bytes). Incrementing in steps of two starting at address 0 calls out two bytes from successive addresses. Additional conditions that enable the +2 Operation are:

a. Gate M103 (AAC220) allows a+2 function during the EXECB cycle for all nonimmediate instructions except CMC. (INDXB* input inhibits the +2 function during power restart.)

b. In the Test Jump Class of instructions, a Jump on Condition can be performed. This is a 2-word instruction and requires testing of the Condition Status Register (CSR) to determine the specified situation for the Jump on Condition; that is, the CSR is tested for equality, carryout, etc. If the test is successful, a +2 Operation is performed.

c. A JSR instruction (OPD15) or an Increment By Two instruction (OPD12) enables the control signal during EXECA via a high output from M121 (AAC224).

d. M120 is enabled by a high EXECA signal to pin 13. This signal indicates the start of the Execute cycle of an instruction at which time a +2 Operation is needed for JSR and IN2 instructions.

e. M103 (AAC212) receives certain inputs during the Auto Exec cycle. Presence of a low Compare Cursor signal (AACP20) or two low signals (EXTB and EXTF) from the Extension flip flops in the State Counter enable M103, which in turn enables M120.

M84 (+1AAU) generates a control signal that initiates the +1 Operation in the AAU. Normally, a +2 increment is called for; however, some conditions require a+ 1 increment. The conditions occur during the Execute Cycle and Boot State. M84 (+1AAU) is one half of a dual 2-wide, 2-input and-or-invert gate. It is enabled (low) when two high inputs are present at either and gate. The presence of the Execute A signal (EXECA) and the Increment signal (OPD10I) enable the +1 Operation. The presence of Boot signals BOOT00 and BOOT02 also enable the+ 1 Operation. During Boot operation, data is presented on a byte basis hence a +1 Increment is required. A Boot character is placed at some address and stored. The next byte is stored at the previous address plus one.

M11 (+4 AAU) generates a control signal that initiates the +4 Operation in the AAU. It is enabled in the low state. During an Instruction B operation, if a test fails, the program increments by four to pick up the next instruction. The +4 Operation is enabled if a high FAIL TEST I signal and a high INSTB signal are present on the inputs of M11.

M9 (AAR/AAU) generates a control signal that enables the Auxiliary Arithmetic Register (AAR) to the Auxiliary Arithmetic Unit (AAU). This operation is performed during a Compare Cursor instruction (AACC12) or a Refresh Cycle (signal REFB). In the case of the Compare Cursor instruction,

timing is very critical. Data in the MDR and CUR are compared and the results placed in the register that initially changes the data going into the AAU Adder.

M53 (STRBAARI) generates the strobe signal for the Auxiliary Arithmetic Register (AAR). A Register Reset signal (REGRST) to pin 3 enables the strobe. The AAR is also strobed at T7 and T17. Time T7 is used on instructions like Increment during which an operation is performed in the AAR and the results are sent back to the MDR for the Read/Restore cycle. During some instructions, the T7 strobe is in a "don't care" state. The associated gates are M39 (RFINH) and M39 (STRBAAR). A low T17I signal to M39 (STRBAAR) enables the strobe. A high T7 signal anded with a high REF01 signal to M39 (RFINH) also enables the strobe.

M88 generates two signals that indicate a Successful Test operation or a Failed Test operation. The nor gate on the left is enabled in a low state which indicates a Successful Test; the nor gate on the right is enabled in a low state which indicates a Failed Test operation. The associated gating (M72 and M25) accept inputs associated with Jump On Condition, Compare and I/O Testing instructions. M88 is a dual 2-wide 2-input and-or-invert gate. M72 is a quad 2-input exclusive-or gate. The output of each M72 exclusive-or gate is connected to the input of a different and gate in M88. Each M72 gate is enabled when one and only one of its inputs is high. A variety of input signal variations can enable M88. The IOTEST gate (M25) is enabled when its three input signals are high. This requires that an I/O Instruction is present (pin 13); MDR08I is high (pin 2) denoting that it is a Test I/O; and MDR09I is high (pin 1) denoting that it is not a Read I/O or a Wait I/O.

5.3.7 Arithmetic Unit Control

The logic that controls the Arithmetic Unit (ARU) is shown on sheet 12. Refer to the left side of the sheet. M107 (ACRARU) generates a control signal that enables the Accumulator Register (ACR) to the Arithmetic Unit (ARU). An Add instruction enables the loading of the ARU so that the addition is performed during the Execute cycle. This is accomplished at M125 (ACRA20) by anding an Add instruction (OPD2I) with an EXEC signal. Both signals must be

high. An Add Immediate instruction can affect the same action directly because the Add Immediate instruction (OPD18) is connected to pin 1 of M107 (ACRACU).

One step in the process of getting information to the ARU for arithmetic processing is transferring data from the Memory Data Register (MDR) to the Arithmetic Bus (ARB). M92 (MDRARB) generates a control signal that enables the MDR to the ARB. M107 (MDR*ARB) generates the signal for enabling the complement of the MDR (MDR*) to the ARB. The instructions that enable these control signals must be byte class because the ARB has eight bits. The MDR-to-ARB control signal is enabled directly by all the Immediate class instructions, except Subtract Immediate. An And, Or, Add or Load Instruction anded with an EXEC signal also enables the MDR-to-ARB signal. This is accomplished with gates M77 (ARCM22) and M125 (ARCM12). The MDR*-to-ARB control signal is enabled directly by a Compare and Jump On Condition instruction or a Subtract Immediate instruction. A Subtract or Compare instruction anded with an EXEC signal also enables the MDR*-to-ARB control signal.

M60 (LOW/ARBM) clears out bits 6 and 7 during a transfer of data from either the Line Register (LIR) or the Character Register (CHR) to the Accumulator Register (ACR). The LIR and CHR contain only 6-bits each; and the ACR contains 8-bits. Dropping bits 6 and 7 insures that the exact contents (bits 0 through 5) of the LIR or CHR are contained in the ACR.

M43 (IOARB) generates a control signal to enable the Data In Bus to the Arithmetic Bus. Data entering the Terminal via a Controller circuit board comes in via the Data In Bus and is routed to the ARB. Data enters during the Boot cycle. The Controller raises the Boot line and when a character is available the system enters the Boot Wait state. In this condition, the State Counter generates a Boot Wait signal (BTWAIT). A low BTWAIT signal to pin 13 of M43 enables the control signal. Another enabling signal is provided by M56 (ARCI/O) if an acknowledged Read I/O or Write I/O is present. This requires three high input signals to M56 (ARCI/O): I/O (OPDI25), RIO or WIO (MDR09*) and I/O ACK (ACKI).

M57 (STRBCSRI) generates the strobe for the Condition Status Register (CSR). The associated input gating permits several conditions to enable the CSR strobe. A high CSC24 signal anded with a high T11 pulse enables the strobe via M42 (CSC14) and M56 (STRBCSR). The CSC24 signal is generated by gate M25 (see top left of sheet 12). The strobe is generated by anding the output of M107 (CSC20) with a high T7 pulse at M42 (CSC10). M107 is enabled by any one of three low input signals: an Increment instruction (OPD10); an Increment-by-Two instruction (OPD11); or a Decrement instruction (OPD12). Another enabling condition is provided by the anding of the Compare Cursor instruction, EXEC signal and a T16 pulse (all high signals) at gate M124 (CSC12). The strobe is also generated directly by a high Register Reset signal to pin 8 of M57 (STRBCSRI).

M26 (AAU/CSR) generates a control signal to enable the Auxiliary Arithmetic Register (AAU) to the Condition Status Register (CSR). The signal is enabled by a low Compare Cursor signal to pin 5 of M26. It is also enabled by a low Increment, Increment-by-Two, or a Decrement instruction via M107 (CSC20) and M108 (CSC21) to pin 4 of M26.

M45 (ACR/ARB) generates a control signal that is used during the Boot cycle to shift the four least significant bits of data to the four most significant bits of the Accumulator Register. This control signal is enabled by a low signal to either input of M45. One signal is OPDG09, which is the 4-bit shift signal from the Generic Op Code Decoder; the other is the BOOT SHIFT signal from the Boot State Counter.

5.3.8 Real Time Clock Module

The Real Time Clock (RTC) module is shown on 005-07-01, sheet 13. Although the RTC is not physically an I/O controller, its interface appears as a controller to a programmer. The clock rate is 15 Hz. The RTC interrupt has the highest priority and occurs once every clock cycle or every 66.7 milliseconds. All the I/O Controllers receive their Interrupt Select signals from the RTC. The Interrupt Select is a priority process that loops through all the I/O Controllers. Because the RTC is the highest priority interrupt, it inhibits the Interrupt Select signals to the I/O Controllers when its interrupt has been raised. The RTC also sends an Acknowledge signal to the I/O Bus just like any other I/O Controller.

M111 (RTCMSK) is a flip flop that masks or unmasks the RTC interrupt. Its inputs are conditioned by M112 (UNMRTC) and M112 (MSKRTC). With a low FUN00 signal to pin 5 of M112 and a high FUN01 signal to pin 8 of M112, the inputs to M111 (RTCMSK) are J= 1 and K = 0 (when CONT15 is present). The next T9 pulse sets M111. The RTC Ready flip flop M111 (RTCRDY) is toggled by the RTC clock input. With both M11 flip flops set and the Interrupt Select signal enabled, the RTC Interrupt is raised at the output of M113 (INTRTC) and the RTC Interrupt Select signal to the I/O Controllers is inhibited at the output of M96 (RTCSELI). The RTC Acknowledge signal is generated at M2 (AKDRTC). It acknowledges only when its special address signal (CONT15) and the proper I/O Type signal (MDR09I) are enabled to the input of M112 (READRTC).

When M111 (RTCMSK) is in the reset state (J = 0, K = 1), the RTC Interrupt is inhibited and the RTC Interrupt Select signals are passed along to the I/O Controllers.

A low RESET signal clears M111 (RTCMSK) directly; and through a gating network, input to pin 9 of M96 (CLRRTC), clears M111 (RTCRDY) which inhibits RTC Interrupts. The process also occurs when Terminal power is energized.

5.3.9 Interrupt Controls

The logic that controls the system interrupts is shown on 005-07-01, sheet 14. A special matrix block (STB4) is hardwired on the Control Board. The matrix block configuration is the same for all Terminals used in a specific application. Connectors are provided for a maximum of eight I/O Controllers. Each Controller is dedicated and is wired in with an interrupt line that is fixed with relation to the physical connector. The Controller address is not related to the position or connector number. Any controller can have any address number but the associated interrupt must have the same number as the address. For example, a Controller plugged into connector 1 can have Address 6 but it must have Interrupt 6. This provides the programmer flexibility in defining addresses in the software.

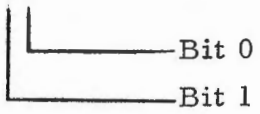
Use of a separate Interrupt line for each controller enables the TPU to sense which controller is interrupting. The TPU will not receive an

interrupt from any controller that has masked interrupts. It will not receive any interrupts if the interrupts have been disabled due to a System Reset, execution of the Disable Interrupts instruction, or servicing of a prior interrupt. If the controller is unmasked and the TPU enabled, the TPU can be interrupted as soon as the current instruction terminates. At this time, the TPU examines all the controller interrupt request lines and, if none are set, the next instruction is fetched. Otherwise, interrupts are disabled and the highest priority is selected.

Two words (four bytes) of core memory are reserved for each controller (or device) for status storage which is part of the Auto Exec feature (reference Section VII of the SPD 10/20 Programmer's Reference Manual). When enabled, each device must generate its associated address, which is given in hexadecimal notation. In a 2K system, controllers 0, 1 and 2 should generate codes FF0, FEC and FE8, respectively. All these special addresses contain a hex F in the MSB, which means that its binary equivalent is 1111. Whenever a special address is enabled, the four most significant bits (11 through 8) are all 1's. Bits 7 and 6 are always 1's also because in all addresses the second hex character (bits 7 through 4 of the address) is either F (1111), E (1110) or D (1101).

Assume that Controller 0 is the one being considered. It should generate address FF0. As described above, bits 11 through 6 are all 1's. The address will be complete if 1's are picked up in bits 5 and 4, and 0's in bits 3 through 0. The first six bits (11 through 6) are picked up by inverters M8 (see top left of sheet 14). Bit 5 will be cleared if Interrupt 7, 6 or 5 is true. Bit 5 is obtained at the output of M12 (MABSP05); M66 (SPS05I) and M1 (SPS05) are associated input gates. Bit 4 is obtained at the output of M3 (MABSP04) and is inhibited by the oring of several addresses. Bits 3 and 2 are generated by the oring of several addresses. They are obtained at the outputs of M2 (MABSP03) and M2 (MABSP02) through the associated input gating. Bits 1 and 0 are always 0's because all the special addresses have an even number; that is, the last digit is even as shown below.

Controller Number	Least Significant Hex Character	Binary Equivalent
0	0	0000
1	C	1100
2	8	1000
3	4	0100
4	0	0000
5	C	1100
6	8	1000
7	4	0100



Special address FF8 is identified as Interrupt Program Save Area and is used to save the status of the interrupted program.

M94 (INTMASK) is an Interrupt Mask flip flop that controls the generation of the Interrupt Select clock signal from M94 (INTSEL). Normally this signal is supplied to the Real Time Clock and the other I/O Controllers. Certain conditions require that the interrupts be masked which disables the Interrupt Select clock. The gating shown below the M94 flip flops conditions their inputs and controls generation of the Interrupt Select clock signal. A WAIT instruction or entry into Auto Exec cause generation of the Interrupt Select clock to be inhibited.

M50 (RETURN) generates the special address for the Interrupted Program Save Area. A high COMP INT signal to pin 4 of M50 (RETURN) enables the address. Another enabler is a high EXTX signal anded with a high INTERRUPT I signal to M50 (NTC30).

5.3.10 Controller Decoder and Wired Option Matrix

Logic diagram 005-07-01, sheet 15, shows the Controller Decoder and Wired Option Matrix. It consists of a 4-line-to-16-line decoder (ADD00 through ADD15) and two special wired matrix test blocks STB-13 and STB-14. The decoder inputs are MDR00* through MDR03*; and the outputs are ADD00 through ADD15. It is enabled by simultaneous low inputs to pin 18 (EXEC)

and pin 19 (OPD 25). The only dedicated output is ADD 15 (pin 17) which is always assigned to the Real Time Clock. The configuration of the jumpers that plug into the test blocks determine the I/O Controller address assignments.

5.3.11 Control Line Drivers

Logic diagram 005-07-01, sheet 16, shows the inverters and drivers used for the incoming signals on the Control board. The inputs on the bottom row are all timing phases (T2, T3, etc.). Some of the inputs on the upper row are Memory Data Register bits from the Data Flow board. Where additional buffering is required, type 7440 dual 4-input positive nand buffers are used but each element is connected as an inverter. The other signals are handled by type 7404 hex inverters which have a single input.

5.4 MEMORY ELECTRONICS

5.4.1 Introduction

The core memory stack and associated electronics are located on two circuit boards. The Memory Electronics board, located in slot 10 (see Figure 5-7), contains the X and Y drivers and logic, inhibit logic and memory sense logic. The Memory Stack board, located in slot 11 (see Figure 5-8), contains the memory core stack and sense amplifiers.

Figure 5-9 is a simplified block diagram of the Memory Electronics board and Memory Stack board.

The logic for the Memory Electronics board is shown in drawing 001-06-01 (5 sheets). The logic for the stack sense electronics is shown in drawing 001-12-02 (2 sheets).

Paragraph 5.4.2 is a general discussion of the memory organization and operation. Its purpose is to orient the reader prior to entering the detailed discussion of the memory system.

5.4.2 General Discussion of Memory Organization and Operation

The core memory used in the SPD 10/20 terminal is a 3D 4-wire coincident-current type. The memory capacity is 2048 words of 16-bit length.

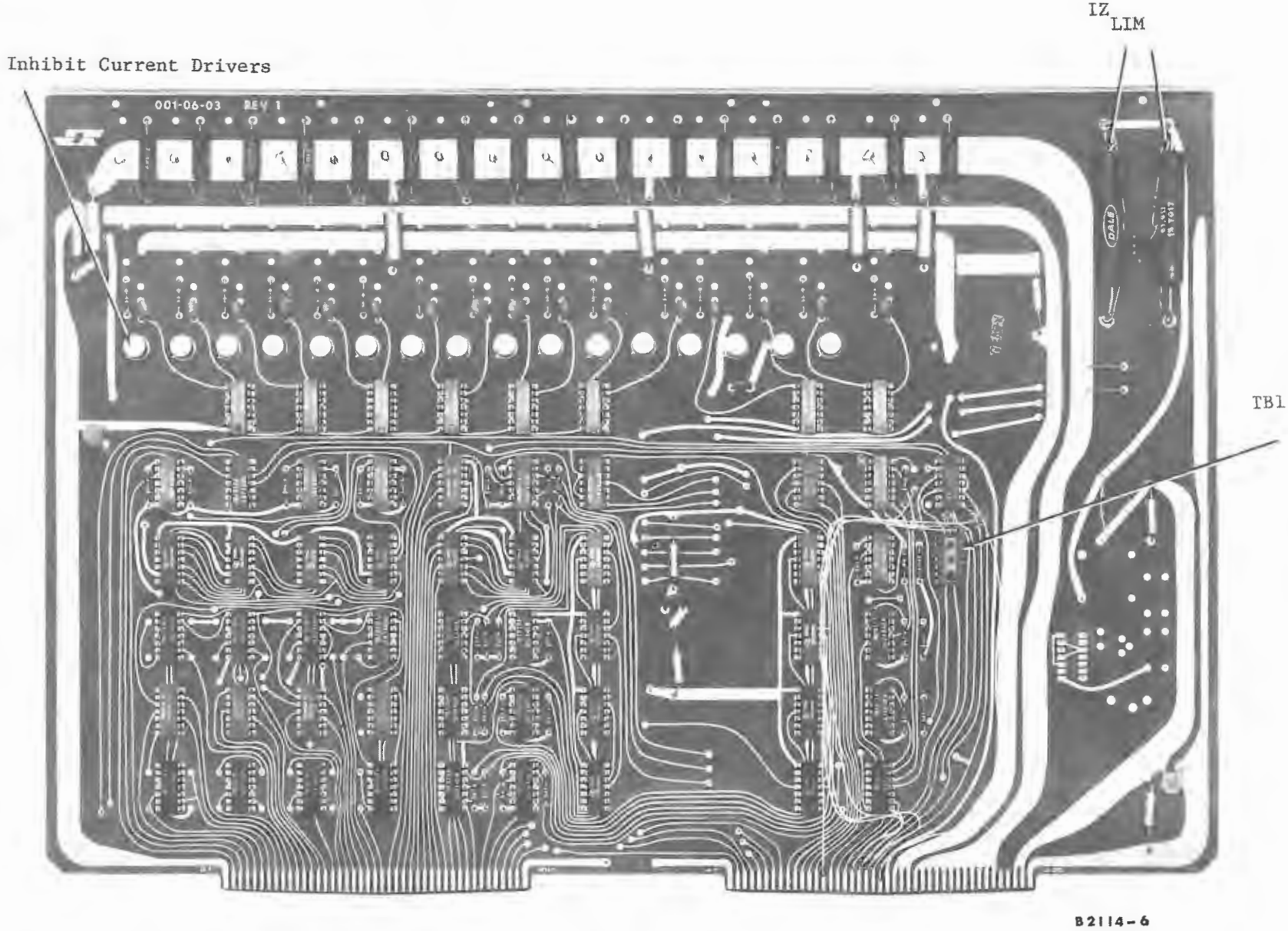


Figure 5-7. Memory Electronics Module

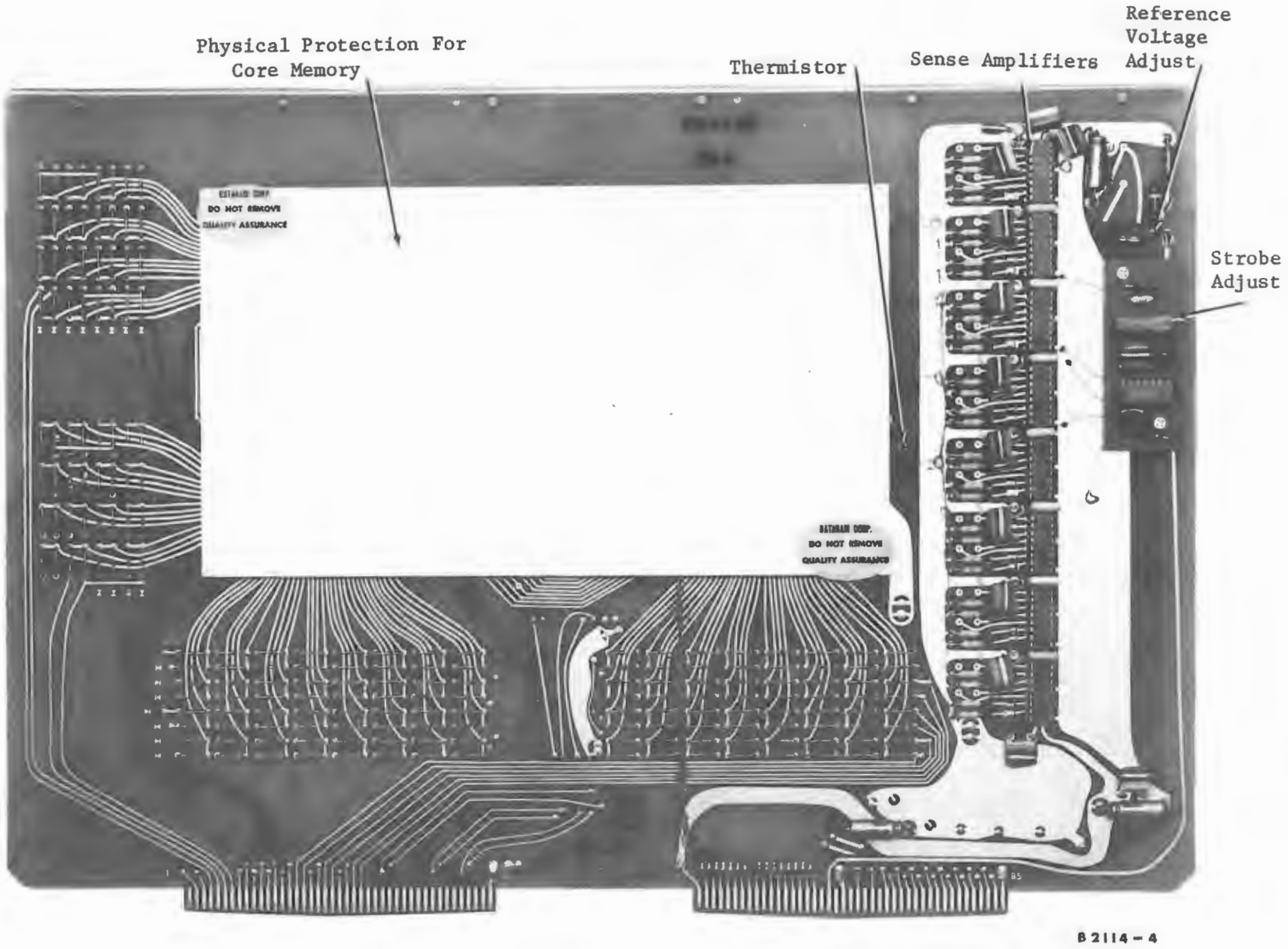


Figure 5-8. Memory Module

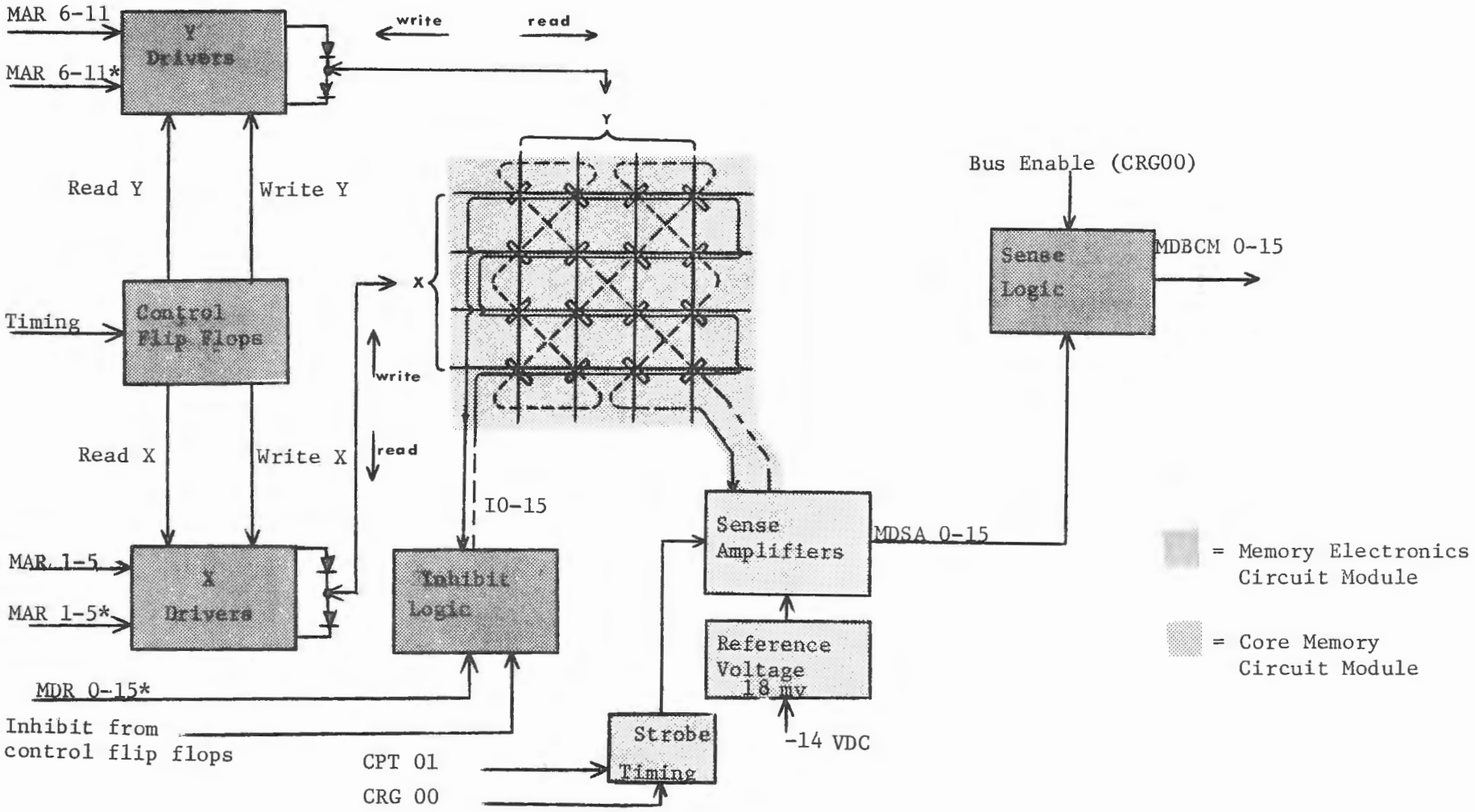


Figure 5-9. Simplified Block Diagram, Memory System

The sixteen bit-planes are arranged in a 4 x 4 pattern. Each bit-plane consists of a 32 x 64 core matrix (2048 cores) arranged in 32 rows (X) of 64 columns (Y) each.

The cores in each row are threaded with a wire called the X-select line. It is continuous through the corresponding row of each bit plane. The cores in each column are also threaded with a wire called the Y-select line. It is continuous through the corresponding column of each bit plane. Any pair of X and Y lines intersect at only one core per bit-plane; however, the same core on all 16 planes is intersected. These lines are used to select the particular core location being addressed. Two additional lines are strung through all cores in a plane. One is the inhibit line that passes through all cores in a plane and is run parallel to either the X lines or the Y lines. The other is the sense line that passes through all cores in a plane in a predetermined pattern designed to eliminate noise pick up. These four wires, X, Y, inhibit and sense, allow information to be written into and read out of any individual core in a plane.

The actual storage of information takes place in the ferrite core and is based on the ability of the core to respond to bidirectional magnetization, which is affected by bipolar current flow in the X and Y select lines. The mass of a core is very small and very little magnetizing force is required to switch the core. The resulting switching speed is very fast; approximately 450 nanoseconds for a 30 mil core.

A core is selected by sending half current ($I_{m/2}$) pulses through a particular pair of X and Y lines. Several cores receive either an X- current pulse or a Y- current pulse, neither of which is sufficient to switch the core. Only the core at the intersection of the X and Y lines receives both pulses. The pulses are additive and produce enough magnetic force to switch the state of the core.

A typical memory Read/Write cycle is discussed in general terms.

1. Assume that the proper core location has been addressed (X and Y lines selected).

2. A Read pulse is applied to the X and Y lines. The Read current is always in the direction that would magnetize the core in the one direction.

3. If the selected core was previously magnetized in the one state, the core does not switch and the sense electronics detects a one. If the core was previously magnetized in the zero state, the Read current switches the core. This causes a flux change which induces a voltage pulse in the sense line. Through suitable electronics, this pulse is detected as a one.

4. The Read operation has destroyed the stored information and it must be restored. Although destroyed in the core, the information that has been read out is temporarily stored in a register. It is transferred from the register back to the core during the Write operation.

5. During the Write operation, the X and Y lines are pulsed with Write currents that are of opposite polarity to the Read current pulses. This tends to magnetize the core in the zero direction.

6. If the Inhibit current is not turned on, the core switches back to the zero state. If a one is to be restored, the Inhibit line is driven with a half-current pulse that is of opposite polarity to one of the Write currents. This cancels out either the X or Y Write pulse so that not enough magnetizing force is produced to switch the core. The core remains in the one state.

Obviously, a considerable amount of circuitry is required to implement the Read/Write cycle. It is discussed in the subsequent paragraphs.

5.4.3 X and Y Drivers and Associated Logic

The X and Y drivers and associated logic are shown on drawing 001-06-01 (sheet 4 for X and sheet 5 for Y). The circuits for the X and Y drivers are very similar. The Y drivers are discussed because the logic for generating the READ/WRITE timing signals for both X and Y drivers is shown on the drawing for the Y- drivers (sheet 5).

Eight drivers are used and they are identified as M7, M8, M16, M17, M25, M26, M34 and M35. Each one is a Texas Instruments Type SN75324 Memory Driver. The SN75324 is a monolithic memory driver with decoding inputs. Figure 5-10 is a simplified functional diagram of the device. The unit consists of four fast, high-current switches controlled by seven logic inputs. Two of the switches control current from the source collector terminal to the outside (Source A and Source B): the other two sink current into the ground terminal (Sink A and Sink B).

The RC network (R82, R136 and C37 on the right side of sheet 5) provides limiting and wave shaping to provide optimum drive current. The use

TRUTH TABLE

INPUTS							OUTPUTS			
Device Select			Switch Pair		Source/Sink					
E	F	G	A	B	C	D	Source A	Sink A	Source B	Sink B
0	X	X	X	X	X	X	off	off	off	off
X	0	X	X	X	X	X	off	off	off	off
X	X	0	X	X	X	X	off	off	off	off
1	1	1	1	0	1	0	ON	off	off	off
1	1	1	1	0	0	1	off	ON	off	off
1	1	1	0	1	1	0	off	off	ON	off
1	1	1	0	1	0	1	off	off	off	ON

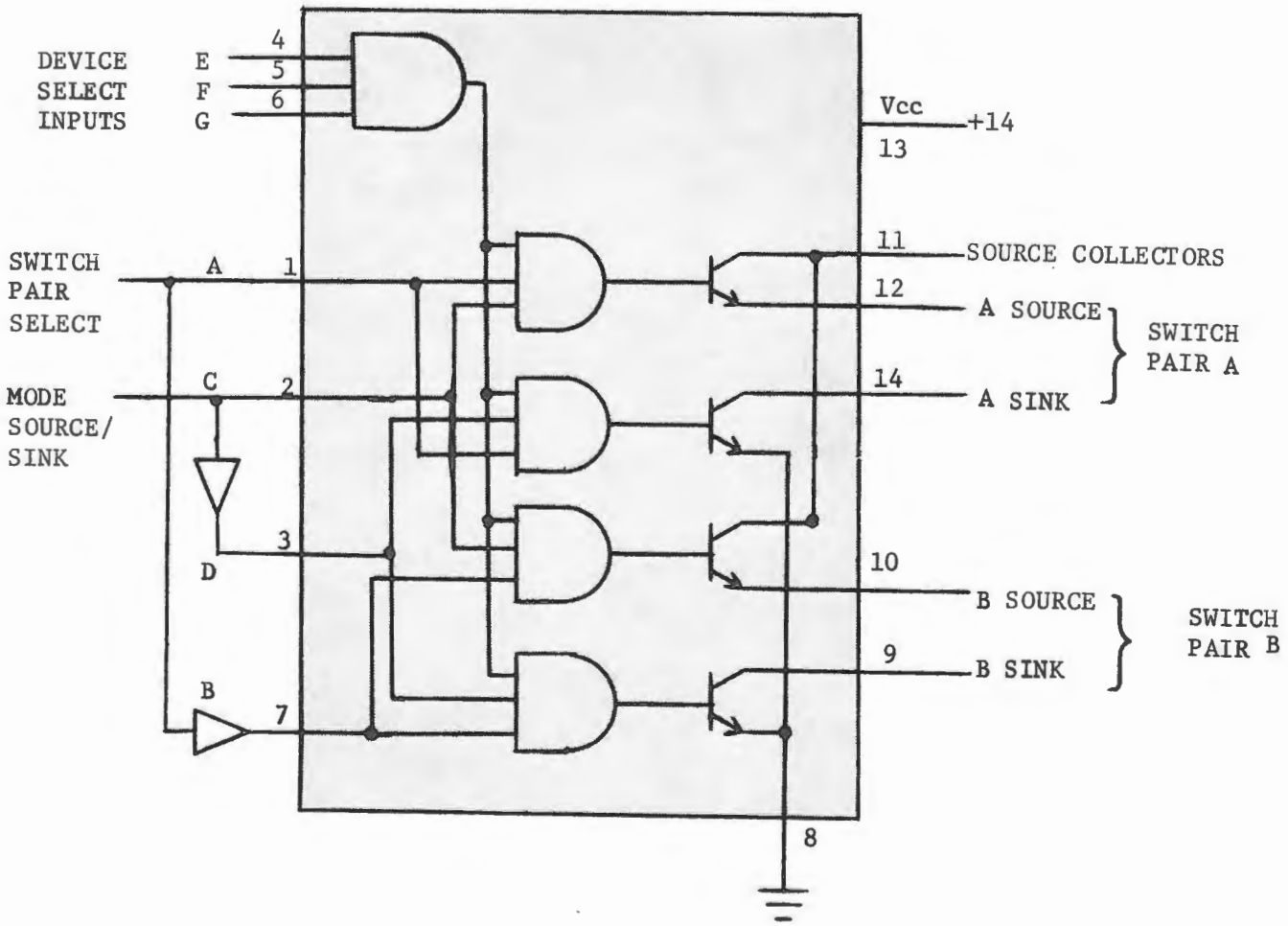


Figure 5-10. Simplified Functional Diagram and Logic Table for SN 75324 Memory Driver

of +25V coupled with C37 and R136 insures a rise time of approximately 100 nanoseconds. Current limiting is provided by R82. Diode CR2 clamps the source collectors of the drive IC's to +14V when they are inactive. A source and sink are paired and are selected as output switch pair A or B by inputs A and B respectively. Inputs C and D are used to select the mode of operation; that is, source or sink. Logic inputs E, F and G are used for device selection. External logic allows only one switch per IC to conduct at one time. The unit will overheat if more than one switch at a time carries memory current. The Truth Table in Figure 5-10 also shows which logic inputs (A-G) must be high to enable a specific switch. The use of positive logic is assumed.

The source/sink arrangement permits bipolar current flow, which is required to perform a READ/WRITE operation.

The 64 Y-lines are selected through a matrix of 8 x 8 driver switches. M8, M17, M26, and M35, the drivers for lines YPD/ND0 through YPD/ND7, are connected to the diode end of the memory stack. All PD lines are connected to source switches which are turned on during READ time, while all ND lines are connected to sink switches which conduct current during WRITE time. The return lines YR0 through YR7 on the other end of the matrix are driven by circuits M7, M16, M25, and M34. At these drivers the sources and sinks of each switch pair are connected together. During READ the sink of the return switch pair turns on, thus current flows out of the source of the PD driver through the memory stack diode, the selected Y-line into the sink of the return driver. Current flows in the opposite direction during WRITE, i. e., out of the source of the return driver through the selected Y-line, through the stack diode, into the sink of the ND driver.

The X-axis has 32 lines and they are selected through a similar matrix which has only 4 PD/ND pairs, however.

The switch selection inputs of the drive IC's, device selection inputs E, F, and G and switch pair selection inputs A and B, are driven through SN7440 buffer gates and pull-up resistors from the MAR outputs and their complements. MAR bits 1 through 5 select the X drivers while bits 6 through 11 select the Y drivers.

An additional enabling level is needed to turn on the PD/ND drivers. The input signal ENABLE (Pin A29) must be true (low) to generate the two

logically equivalent signals WAITA and WAITB (out of pins 6 and 8 of M36). The ENABLE signal is generated by the Control board and will prevent X and Y current flow when the processor is in the WAIT state.

The READ and WRITE timing signals are generated by 2 R-S flip flops (latches). Refer to the upper right of sheet 5 (gates M9, M18, and M27). The READ latch, M9 Pin 8 and M27 Pin 8, parallel by M27 Pin 6 for added drive current, is set by CPI20 (CPT20, low truth) and cleared by CPI07 (CPT07, low truth). Similarly, CPT10 sets and CPT16 clears the WRITE latch which is formed by gates M9 Pin 12 and M18 Pin 8, paralleled by M18 pin 6, again for added drive current.

In addition the signal PWRESET, which the Control board generates during the power turn-on sequence, also clears both the READ and the WRITE flip flops. Thus the logic of the memory is in a known state before memory power (+14V and +25V) is turned on.

5.4.4 Inhibit Logic and Drivers

The inhibit logic and drivers are shown on drawing 001-06-01, sheet 3. There are 16 drivers: one for each bit plane. An inhibit driver is turned on whenever a one is to be restored in the memory during the Write cycle.

All drivers are identical. A typical driver is shown at the top center of the sheet, identified as Circuit 0. It is constructed with discrete components. The inhibit current is taken from the collector of transistor Q1. During operation, the output current is limited by resistor R65. The transistor is protected from damage during current turn off by diode D3 which clamps its collector to +14V. Capacitors C18-C22 provide instantaneous current storage for the inhibit drive current. Considering that a driver draws 300ma, the +14V supply can experience a large demand, if all 16 drivers are turned on simultaneously.

The base of the driver transistor Q1 is connected to the output of buffer gate M47 (pin 8) via the parallel combination of resistor R1 and capacitor C1. The signal from this gate turns on the inhibit driver. Gate M47 is a type SN74H40 high speed buffer. The control logic must be buffered to generate a signal that is large enough to drive transistor Q1. All the inputs of M47 are tied together which makes it perform like an inverter. A high output from pin 8 of M47 turns on Q1.

The control logic for each driver consists of a 2- input nand gate that accepts a bit from the Memory Data Register and a timing signal called B INHIBIT. Each nand gate is connected to a different bit from the Memory Data Register: MDR00* through MDR15*. These bits are obtained from the $\overline{Q}$ side of the MDR latches. The timing signal (BINHIBIT), which is common to all drivers, is generated by M45 and M9 which are connected as a simple latch circuit. Gate M45 is the set side which is controlled by input clock pulse CPT09. A positive CPT09 pulse sets the latch and produces a high output at pin 6 of M45. If MDR00* is high (representing a one stored in the MDR), M38, pin 11 is forced low and inhibit driver IOA is turned on. Any other input nand gates that sense a high MDR* bit are also turned on. The latch is reset when clock pulse CPT17 goes high. This produces a low at the output of M45, pin 6 which disables input nand gate M38 (pin 11 is high) and turns off inhibit driver IOA. Any other inhibit drivers that were on are also turned off. Refer to the timing diagram shown on Figure 5-11.

5.4.5 Memory Stack Sense Electronics

The memory stack sense electronics consists of the sense amplifiers, sense amplifier strobe generator and reference voltage circuits.

Sixteen sense amplifiers are used: one for each bit plane. They are Texas Instruments Type SN7524, which are dual packages. Eight packages, identified as E1 through E8, provide 16 sense amplifiers. A typical package (E1) is arranged as follows: The analog inputs S_0 (pins 2 and 3) and S_1 (pins 6 and 7) are twisted pairs from the sense windings from two bit-planes. The associated digital outputs are MSDA0 (pin 12) and MSDA1 (pin 14) which are sent to the sense logic on the Memory Electronics board. Each input has a pair of termination resistors (R1 and R2) connected to ground. A capacitor (C26) is connected across the input lines only if a Dataram memory stack is used. The strobe signal is connected to pins 11 and 15. The reference voltage for both amplifiers is connected between pin 4 (reference) and pin 5 (reference ground). Pins 9 and 13 are connected to ground. An external capacitor (C1) is connected between pin 1 and ground to avoid oscillations of the internal reference amplifier. Capacitor (C9) is connected between pins 4 and 5 to decouple the reference voltage.

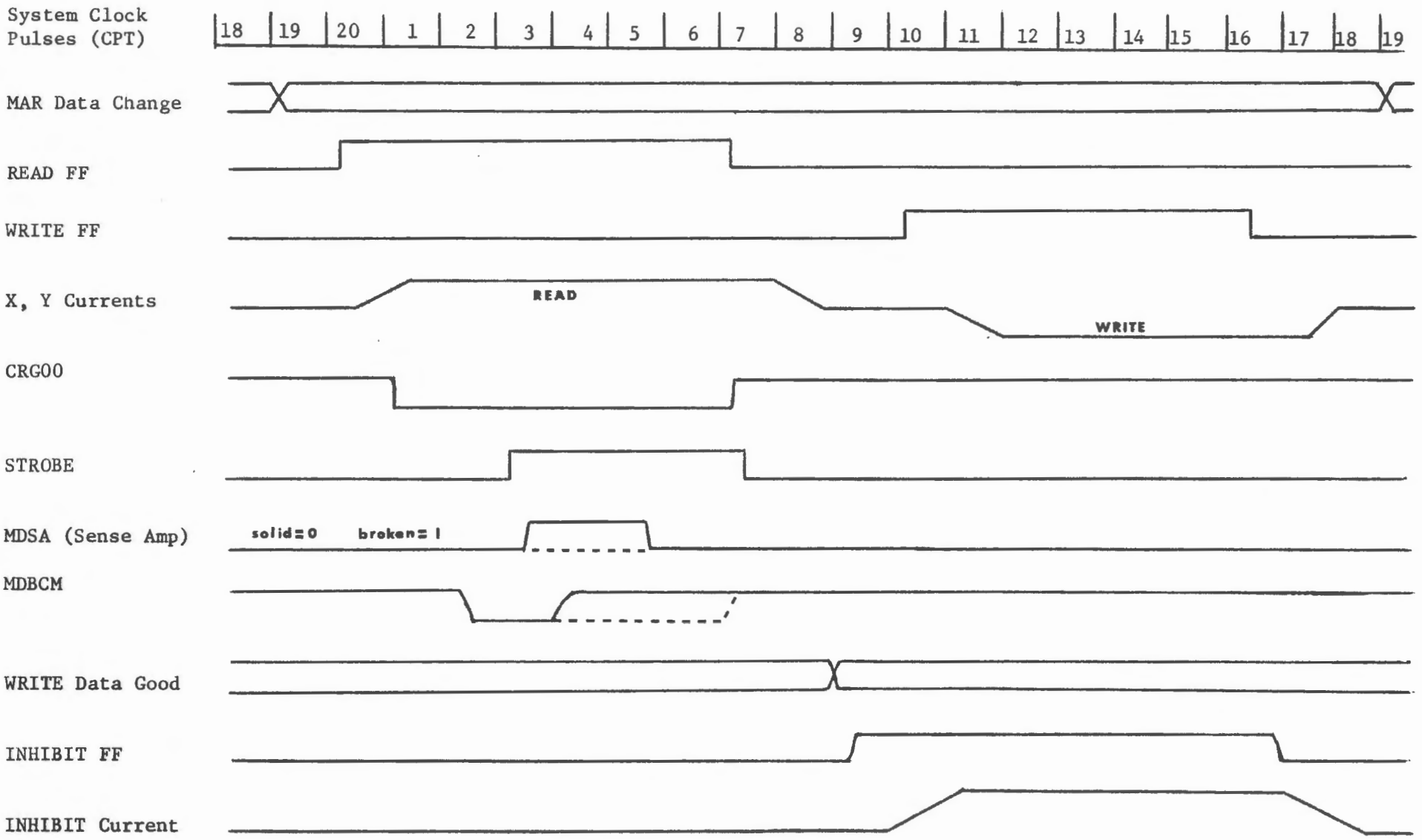


Figure 5-11. Memory Timing

Basically, if a core is switched during the Read operation, a voltage is induced in the sense line and sent to the input of the sense amplifier. It is amplified and compared to the reference voltage. If the sense signal exceeds the reference voltage and the amplifier is strobed (strobe input high), the digital output is high.

The 18 mV reference voltage for the sense amplifiers is obtained from the -14V supply by using a 5.6V Zener diode (D1) and a voltage divider network. Potentiometer R34 is used to adjust the reference voltage level. Capacitor C17 together with capacitors C9-C16 provide decoupling for the reference voltage.

The strobe for the sense amplifiers is generated by the circuit shown in the lower right section of drawing 001-12-02, sheet 2. The circuit performs like a standard monostable multivibrator (one-shot). When triggered, it changes to its unstable state and falls back to its original or stable stage after a period of time that is determined by its RC time constant. Normally, transistor Q1 is on and pins 6, 9 and 12 of E9 are low. A high CRG00 signal to inputs 8 and 11 of E9 produces a low output at pins 10 and 13 of E9. A high CPT01 clock pulse to input 5 of E9 starts the one-shot period. It causes a low output at pin 4 of E9 which turns off transistor Q1. Its collector now holds pin 4 low (via input pin 6) as well as insuring low outputs at pins 13 and 10 (via input pins 12 and 9) for the duration of the astable state of the one-shot. Sometime during the astable state, CRG00 goes low and remains low until the start of CPT06. When the one-shot has timed out, Q1 turns on again and the low inputs at gate E9 inputs 12 and 9 generate a high strobe level output for the period during which CRG00 stays low.

Adjustment of R37 determines the duration of the one-shot astable state and thus controls the beginning of the strobe. During test, the strobe is adjusted to start approximately 20 ns before the peak of the core switching (zero) signal.

5.4.6 Memory Sense Logic

The memory sense logic is shown on drawing 001-06-01, sheet 2. The circuitry accepts the outputs of the 16 sense amplifiers on the Memory Stack board, stores them in a temporary register, and enables them to the Memory Data Bus (MDB).

The logic consists of 16 flip flops and 16 output buffer gates. Type SN7402 quad 2-input positive nor gates are used to construct the flip flops which are simple RS latch circuits. Each SN7402 package provides two flip flops. The packages are identified as M1, M2, M3, M4, M19, M20, M21 and M22. The buffers are type SN7403 quad 2-input positive nand gates. The packages are identified as M10 through M13.

Clock phase TURT1, through M46, keeps the flip flops reset. Just prior to strobing of the sense amplifiers, the reset signal is disabled and the flip flops are now sensitive to any output pulse from the associated sense amplifiers via inputs MDSA0 through MDSA15. At the same time, an enabling signal is applied to one input of each buffer to transfer the output of the sense flip flop to the Memory Data Bus. Shortly after strobing the sense amplifiers, the flip flops are reset and the buffers are disabled.

5.5 TIMING AND REFRESH ELECTRONICS

5.5.1 Introduction

The Timing and Refresh Electronics are contained on one printed circuit board located in slot 14 (see Figure 5-12). The circuitry provides the interface between the Terminal Processor Unit and the Display Unit. It performs two major functions: generation of a system timing chain from the 12.6 MHz output of a crystal controlled oscillator; and the processing and interfacing of control and addressing data from the TPU to the CRT. Selected characters are converted to a 7 x 10 dot matrix which modulates the CRT video circuit and displays the characters on the screen. The characters are refreshed at a rate that prevents image flickering. Circuits are also used to compute the CRT line number and character position on a line. The standard display provides capability for 30 lines of 64 characters per line.

A simplified block diagram of the Timing and Refresh Electronics is shown in Figure 5-13. The logic for these circuits is shown in drawing 005-14-01 (14 sheets) and is divided into the following major functional components.

A. Timing Circuits
   1. 20-phase Clock Timing Unit
   2. Segment Counter, Segment Decoder and Line Counter
   3. State Counter and Horizontal Sync and Blanking
   4. Vertical Sync and Clear

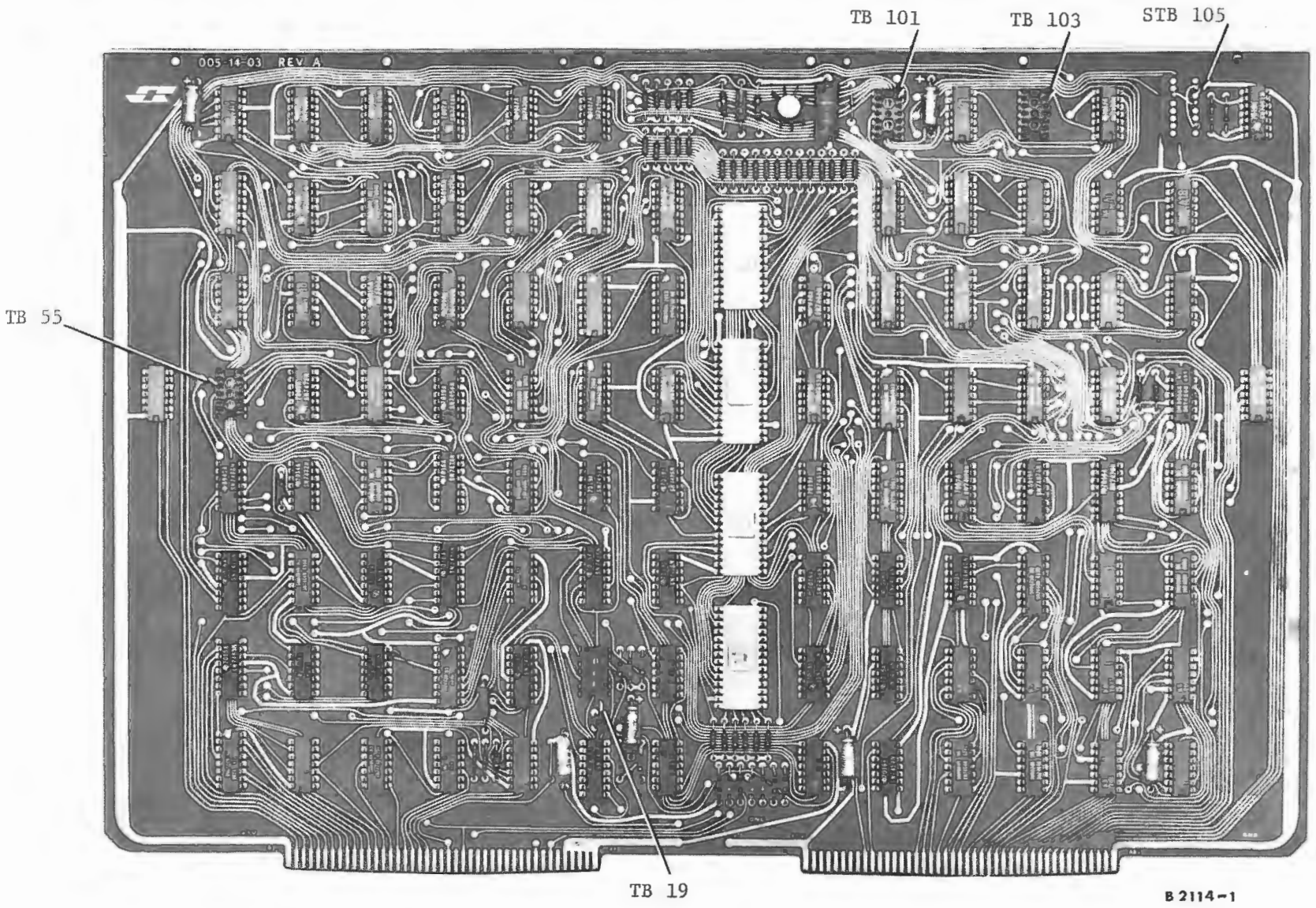


Figure 5-12. Refresh Module Timing Unit

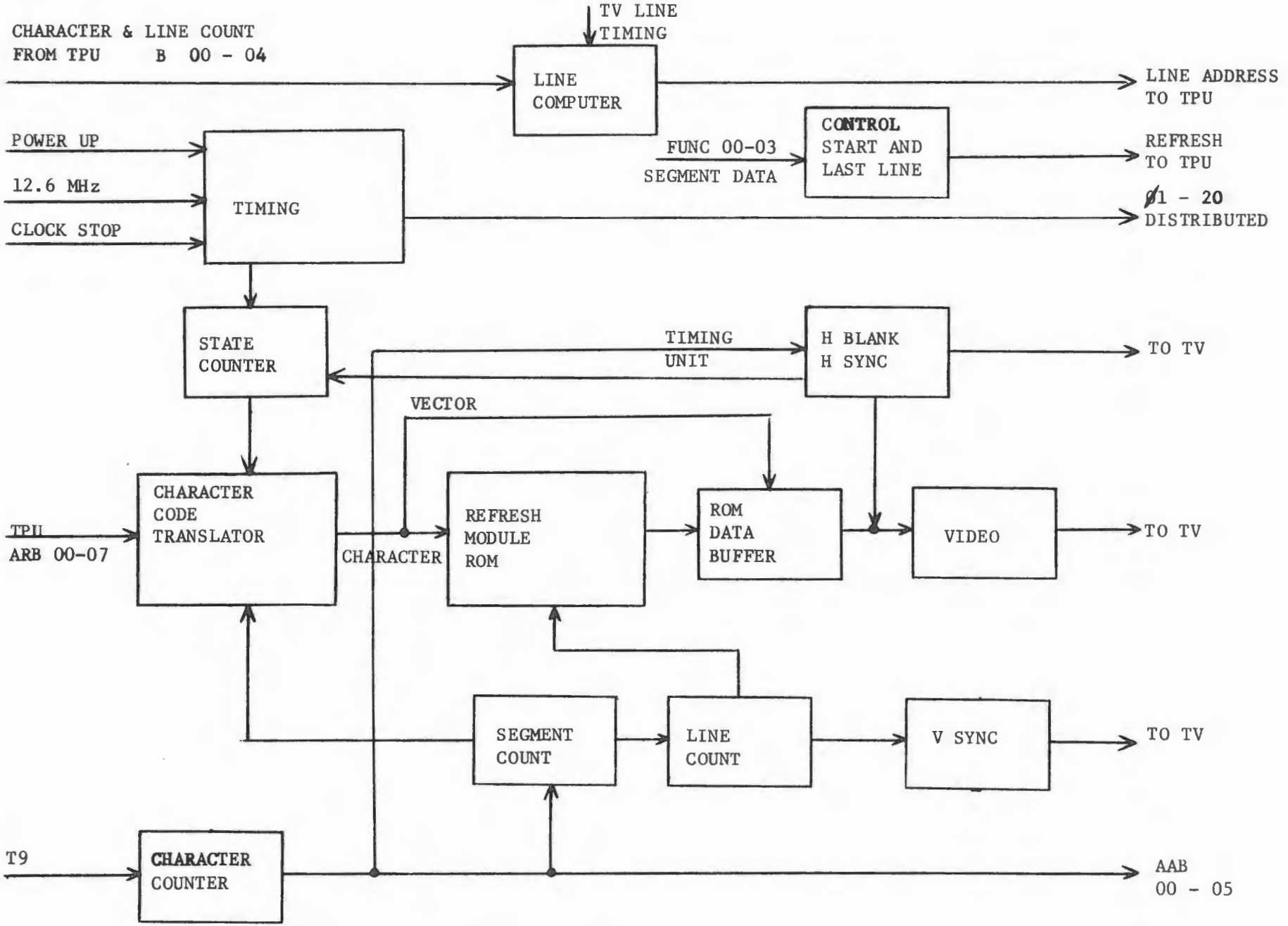


Figure 5-13. Simplified Block Diagram Refresh Module Timing Unit

B. Refresh Circuits

1. Display Control/Start and Last Line Control
2. State Control
3. Line Computer
4. Character Code Translator
5. Video Circuits
6. Read-Only-Memory
7. Character Counter
8. Line Selection
9. Read-Only-Memory Buffer

5.5.2 20-Phase Clock Timing Unit

The 20-Phase Clock Timing Unit logic is shown on drawing 005-14-01, sheet 8. The timing unit register consists of two type 74H76 high speed dual J-K master-slave flip flops and one type 7476 flip flop identified as TURT0 through TURT4 and TURT4A. Flip flops TURT0 through 4 are synchronously clocked by a 12.6 MHz signal that enters via gate M106, pin 1. The other inputs are connected to option block STB105 which is used only in conjunction with the Test Console to disable the clock and enable a single pulse feature from the console. The Q outputs of TURT0 through 4 are used as inputs to the timing unit decoder M39. This unit is a type 7442 4-line-to-10 line BCD to decimal decoder. The 10 outputs are sent to various gating networks to provide the various clock phases used throughout the system. Output 7 is sent to M11 (CP177) not only as a system clock phase but also as a clock for flip flop TURT4A.

Clock stop circuitry is enabled during a power failure or through switch action from the Test Console. Reference gate M68 (CSGST) at the top right of sheet 8. Pin 9 is a level signal from the power supply. When it is true (low), the clock is stopped. Pin 10 is connected to the Test Console stop switch via option block STB105-10.

A group of Clock Stop gates (M41, M54, M66, M67, M68 and M104) provide an ordered sequence of clock shutdown and enabling. In the case of a shutdown, assume M68 (CSGST) is enabled (high) because of a power failure. This signal is anded with CPT 16 at M68 (CSG 21) whose low output sets the RS latch composed of gates CSG22 and CSG22*. The low at pin 3 of CSG22*

disables M41 (CSGT4A) and M41 (CSGT4D) which shuts off timing phases 1 through 9 and 20. Gate M68 (CSG23) is enabled (low) by pin 6 of CSG22 and CPI33. Signal CPT05 is now low so it is inverted by M66 (CPI05) and produces a high at pin 9 of M54 (CSG33*), which is part of an RS latch. M54 (CSG33) is the other part of the latch and its pin 12 is low. This input combination sets the latch. The low at pin 8 of CSG33* disables M41 (CSGT4B) and M41 (CSGT4C) which shuts off timing phases 10 and 11, and 12 through 19.

Assume that the power failure is cleared. The output (pin 8) of M68 (CSGST) is low which puts a low on pin 2 of CSG21 and a high on pin 2 of CSG20. Two signals are available via the timing unit register: TURT4 and CPI66 (time 6 or 16) making time 16. These signals are applied to pins 4 and 5 of CSG20 which, at time 16, enables it. This action plus the previous enabling of CSG21 resets the CSG22*/CSG22 latch. The resulting high at the output of CSG22* enables clock phases 1 through 9 and 20 via gates CSGT4A and CSGT4D. At time 5, via signal CPT05, the other latch (CSG33*/CSG33) is reset and clock phases 10 and 11 and 12-19 are enabled.

5.5.3 Control, Start and Last Line Control

The logic for the control, start and last line control is shown on sheet 2. The upper half of the sheet contains the logic for enabling/disabling the refresh operation, enabling/disabling the cursor, and loading the start line. The refresh enable/disable is controlled by flip flop M43 (RFGEN). The cursor enable/disable is controlled by flip flop M56 (CRENAB). Loading the start line is controlled by gates M30 (STG70) and M57 (STG80). The commands used to initiate and stop these operations are programmable and are implemented by function code signals FUNC00 through FUNC03. The refresh enable signal is FUNC01 and the refresh disable signal is FUNC02. These signals and the address signal are used to condition the J and K inputs of flip flop M43. With FUNC01 low, FUNC02 high and ADDXX low, M43 is set (Q = 1). It is clocked by CPT13. The Q output (pin 8) is sent to the CLEAR input (pin 3) of M31 (DISPLAY). When this signal is high, the logic at the bottom of the sheet generates the refresh signals that are sent to the Control Board. When this signal is low (disable refresh), it clears M31 which in turn clears M45 (REFREQ) and M45 (REFS16) and disables the refresh signals to the Control Board. Signals FUNC03 and ADXX condition the J and K inputs of flip flop M56 (CRENAB).

With FUNC03 high and ADXX low, M56 is set (Q = 1) and the cursor is enabled. M56 is also clocked by CPT13.

The Load Start Line signal is generated by M30 (STG70) and M57 (STG80). When FUNC00 is low, ADDXX is low and clock CPT 13 is high, all the inputs to M30 are high and it is enabled (low output). This signal is inverted by M57 and is sent (high) to sheet 4 to clock the line address 4-bit bistable latch M1.

5.5.4 Line Computation Logic

The line computation logic is shown on sheets 4 and 10. On sheet 4, the TPU sends five bits of data to the line computation logic via the Output Bus. Bits OTB00 through OTB03 are sent to the line address bistable latch M1 which is clocked by STG80 from the Load Start Line circuit on sheet 2. Bit OTB04 is sent to M29 (OBT14) and J-K flip flop M28 (STR04). Bits OTB00 through OTB03 are stored in M1 and feed into M14. M14 is a 4-bit binary full adder. The data from STR00 through STR03 represents the character data from the TPU and it is summed with the actual count of character lines on the CRT (TURL0 through TURL3). The adder outputs plus carry bit are added to the sum of OTB04 and TURL4 and then sent to line drivers M2 and M5 (AABCL06 through AABCL10) that are enabled to the Auxiliary Arithmetic Bus by control signal RMAAABI. These five bits represent the line address which is sent to the TPU.

Sheet 10 shows the segment and line counters M95, M70 and M71. Units M95 and M70 are 4-bit ripple-through counters and M71 is a dual J-K flip flop. Segment decoding is provided by M83 (SDD0X) which is a 4-line-to-10-line decoder with only eight outputs enabled.

Control for the Interlace/Non-Interlace mode is initiated at double inverter M85 (IDI and IDI*) at the lower center section of sheet 10. The inverter outputs are sent to the inputs of M84 (CAG10). The output of IDI is anded with CAG00 from M90 to provide the Interlaced mode (30 lines). The output of IDI* is anded with TURSX to provide the Non-Interlaced mode (15 lines).

5.5.5 Character Code Translator

The logic for the Character Code Translator is shown on sheet 5. The translator input consists of 8-bits from the Arithmetic Bus (ARB00 through

ARB07). This data is the character code which effectively is an address in the Read-Only-Memory (ROM). After passing through a pair of inverters (CCI gates), bits ARB00 through ARB06 are sent to character code gates (CCGXX). Bit ARB07 is sent directly without the double inversion and is used as a blink bit if so optioned. Bits 00 through 06 are sent to gates CCG00 through CCG05. Gates CCG01 through CCG04 are enabled to the ROM input latches (see sheet 7) by a Displayable Character signal from pin 12 of M88 (CCI13). Gate CCG00 is enabled by the same signal but it is sent to M47 (CCG10). Gate CCG05 is enabled by a low Display Character signal from pin 12 of M8 (CCD12). Its output is sent to M47 (CCG15). Bits 01, 03, 05 and 07 are also sent to M58 (CCG16) where they are anded with segment count signals. Bits 00, 02, 04 and 06 are also sent to M72 (CCG17) where they are anded with the same segment count signals.

A displayable character is identified by having bit 05 or 06 low. This condition is detected by M42 (CCD11) which is an exclusive-or gate with bits 05 and 06 as inputs. The gate is enabled (high output) if one bit is low and the other bit is high which is always the case for a displayable character.

M47 (CCG10) and M47 (CCG15) supply signals to the ROM input latches that indicate whether the incoming data is a displayable character or vector information. Both displayable characters and vector information are clocked through the ROM latches and other gating to the CRT video circuits.

Installation of option block STB105 allows blinking of a character or a group of characters. A jumper is installed between pins 5 and 11 of STB105 to obtain the blinking code via M18 (BLINK). A displayable character is lost at the start of each line because M18 is reset by the horizontal sync and a new blink code must be inserted. A blink code does not have to be at the start of a line. If a jumper is installed between pins 6 and 11 of STB105, data bit 07 is used to perform this function and a displayable character is not lost. Blinking rate is 1.88 Hz.

5.5.6 Refresh Video Circuit

The logic for the refresh video circuit is shown on sheet 6. The input to this circuit consists of seven bits (CDR00 through CDR06) from the output of the character decoder in the ROM output buffer circuit. This data is stored

temporarily in a character decode register that is composed of two 4-bit bistable latches, identified as M64 and M50. The input data is clocked to the output by CPI88 which carries Timing Unit clock phases 8 and 18. The clock inputs (pins 4 and 13) on each latch are tied together so that all bits are strobed simultaneously. Two clock phases are used, 8 and 18, to match the odd (phase 9) and even (phase 19) strobing of data into the ROM. Two sets of ROM's are used: one each for even and odd characters.

The latch outputs are sent to gates M37 (CDG30) and M23 (CDG64), which are type 7475 two-input and-or-invert gates. One bit is sent to a separate and gate to be enabled by a separate clock phase signal. For example: CPI11 carries phases 1 and 11; CPI22 carries phases 2 and 12, etc. M37 and M23 each has a single output that is sent to gate M8 (VGG71) of the video enabling circuit. These inputs represent the odd and even character data. The third input to VGG71 is the cursor signal from M9 (CBG10). The output of M8 (VGG71) is anded with the Horizontal Bright signal (H BLANK*) and the Refresh signal (REFSIG) at M8 (BRIGHT) whose output is buffered by M7 (VIDEO) and sent to the CRT as the VIDEO Signal.

The horizontal and vertical sync signals are also brought in and are buffered by M20 (HSYN) and M20 (VSYN). The horizontal sync signal to the CRT is a positive pulse 11.2 μs wide with a period of 64 μs. The vertical sync signal to the CRT is a positive pulse 192 μs wide with a period of 16.6 ms.

5.5.7 Read-Only-Memory and Input Logic

The heart of the Read-Only-Memory subsystem consists of four integrated circuit ROM packages identified as ROM 10, 11, 20 and 21 (see sheet 7). MOS p-channel enhancement mode technology is used in the ROM package. Each package stores 64 characters and each character has a 35-bit matrix (7 x 5) for a total of 2240 bits of permanent memory storage. Two packages are used to provide a full 7 x 10 character matrix: one package generates the top half of the character and the other package generates the bottom half. Two pairs are used: one for odd characters and the other for even characters. This arrangement provides more stable operation because each set of ROM's has a more relaxed duty cycle due to the odd/even character generating cycle.

As shown on sheet 7, the pin identifications on each ROM are interpreted as follows. The inputs marked C_A through C_E are the column select lines which change with the segment counts. The enabling signals are generated by a BCD-to-Decimal Decoder/Driver which is shown on sheet 12. This devices is compatible with the MOS circuits in the ROM. The inputs marked I, through I_7 are the parallel lines for the self contained character address decoder. These inputs change and are derived from the logic shown on the left side of sheet 7. The outputs marked 0_1 through 0_7 comprise the 7-bit character code that is sent to the ROM Data Buffer and subsequently to the video circuits. The same numbered outputs of each ROM pair are tied together because they eventually reach the same video line.

The remainder of the ROM subsystem consists of the logic shown on the left side of sheet 7. Signals CCB10, CCG15, and CCG01 through CCG04 from the Character Code Translator are sent to the input of two sets of latches M75/M60 and M74/M60. Each package is a 4-bit bistable latch. Physically, only three packages are used: M75, M74 and M60. Two bits of M60 are used with M75 to form the Odd Character Register; and the other two bits of M60 are used with M74 to form the Even Character Register. The Odd Character Register is clocked by a phase 9 clock signal. Separate clock signals are shown (CPT09 and CPT09A); however, they are both phase 9 clock signals that are sent from sheet 8 via separate drivers. The Even Character Register is clocked by a phase 19 clock signal. The signal designations are CPT19 and CPT19A and they are implemented in the same manner as the phase 9 signals.

The latch outputs are CCR00 through CCR05 (odd character); and CCR30 through CCR35 (even character). These signals are sent to the ROM via a series of special gates (M34, M48 and M61). They are type 7426 quad 2-input high-voltage interface nand gates for driving MOS inputs. The open collector of each gate is tied to +14V via a pull-up resistor (R1 through R12). The outputs of these gates (CCD00 through CCD05 and CCD30 through CCD35) are connected to the ROM character address decoder inputs I_1 through I_6. These signals plus the line selection signals from sheet 12 (CEGR00 through CEGR09) select the desired character code from the ROM.

5.5.8 ROM Data Buffer

The logic for the ROM Data Buffer is shown on sheet 13.

The input circuitry is on the left and consists of a group of seven and-or-invert gates (M22, M36, M49, M63 and M77). These gates constitute a character decoding network with single outputs (CDR00 through CDR06) that are sent to the Character Decode Register on sheet 6. Each gate has a pair of 2-input and gates (CDG00 and CDG05 each has an additional pair to be discussed later). One input of each and gate is connected to an output signal from a ROM package. They are arranged in associated pairs. Gate CDG01 is typical: ROB16 is connected to pin 10 of the upper and gate and ROB 26 is connected to pin 13 of the lower and gate. Signal ROB 16 is the interconnected output from terminal 0_6 of the paired odd character ROM's 10 and 11. Signal ROB 26 is a similar signal from the paired even character ROM's 20 and 21. Each odd character ROM output is anded with the enabling signal from M65 (CDD10); each even character ROM output is anded with the enabling signal from M65 (CDD20). The extra and gates in M77 (CDG00) and M36 (CDG05) accept vector control signals (CCR00, CCR30, CCR05, CCR35) from the ROM input latches on sheet 7. These control signals originate in gates CCG15 and CCG10 in the Character Code Translator on sheet 5. Each one is anded with an enabling signal from M65 (VDG00) or M65 (VDG30).

As previously stated, the signals for enabling the ROM Data Buffer come from M65 (CDD10) and M65 (CDD20). One leg of each gate is connected to signal RMSCB1 which is a state control signal from sheet 3. A low RMSCB1 signal specifies the state which allows ROM data to be enabled to the Character Data Register (see sheet 6). The actual enabling is accomplished by the TURT4 clock signal via M66 (RMIT4) and M66 (RMIT4I). The TURT4 clock signal is generated in the Timing Unit (sheet 8). It is a symmetrical square wave with a period of 1.6 μs. It is high during the last half cycle. Assume that the first half cycle (low) is received at the input of M66 (RMIT4). The output of M66 (RMIT4) is high and the output of M66 (RMIT4I) is low. The outputs of these inverters (RMIT4 and RMIT4I) are sent to M65 (CDD10) and M65 (CDD20), respectively. Under these conditions, pin 8 of CDD20 is high and pin 12 of CDD10 is low. The state control signal RMSCB1 is low when the system is in Character Mode and it is desired to transfer ROM output data to the Character

Decode Register. Gate CDD20 is disabled and CDD10 in enabled which strobes out the odd character data (ROB11 through ROB17). When clock signal TURT4 goes high during its last half cycle, CDD 20 is enabled which strobes out the even character data (ROB 21 through ROB 27).

The logic at the top right section of sheet 13 is associated with the cursor control. The input gate M104 (CUG 00) has four inputs: Cursor Compare signal CSID21; Cursor Enable signal CRENAB; Blink Signal VPS 51; and Segment Decode Data signal SDD 06. When all inputs are high, M104 is enabled (low) to inputs D_1 and D_3 of 4-bit bistable latch M79. The other inputs, D_2 and D_4 are connected to latch outputs Q_3 and Q_1, respectively. Latch M79 performs a time delay. Two clocks are used with the choice depending on the character position (odd or even). Clock signal CPT 12 enables output Q_1 (CUR 00) and Q_2 (CUR 01); clock signal CPT 06 enables outputs Q_3 (CUR 02) and Q_4 (CUR 03). Outputs Q_2 and Q_4 are anded with CPT 09 or CPT 19 in M78 (CUG 99). The output of CUG 99 is sent to M67 (CUF 10) which is interconnected with M67 (CUF 20) to form a simple latch circuit. The latch is set, generating a Cursor Enable signal (CBG 10 high) when M67 pin 5 is low and M67 pin 1 is high. The Cursor Enable signal is sent to the video circuits (sheet 6) to be clocked with time phases 1 or 11, 3 or 13, 5 or 15, and 7 or 17.

Outputs Q_1 and Q_3 are sent to M22 (CUG88) where they are anded with signals RMIT4I and RMIT4 to provide a cursor control signal CCD 12 that is sent to the Displayable/Non-Displayable circuitry on sheet 5.

5.6 HIGH EFFICIENCY POWER SUPPLY

5.6.1 General

The power supply is physically located below the display monitor. All fuses are visible from beneath the Terminal. Within the chassis are two circuit boards, designated Board A and Board B (see Figure 5-14). The A Board contains the large transformer, designated T3, along with diodes and regulating circuitry. The schematic diagram 001-13-01 illustrates the A and B Board components and identifies them by boxing in all A and B board related components. Figure 5-15 is a simplified block diagram of the power supply. Board A performs a DC to DC conversion utilizing the components mounted upon it. The B Board contains the 5 volt regulation and sensing circuits, the 25 volt regulator and the 14 volt regulator.

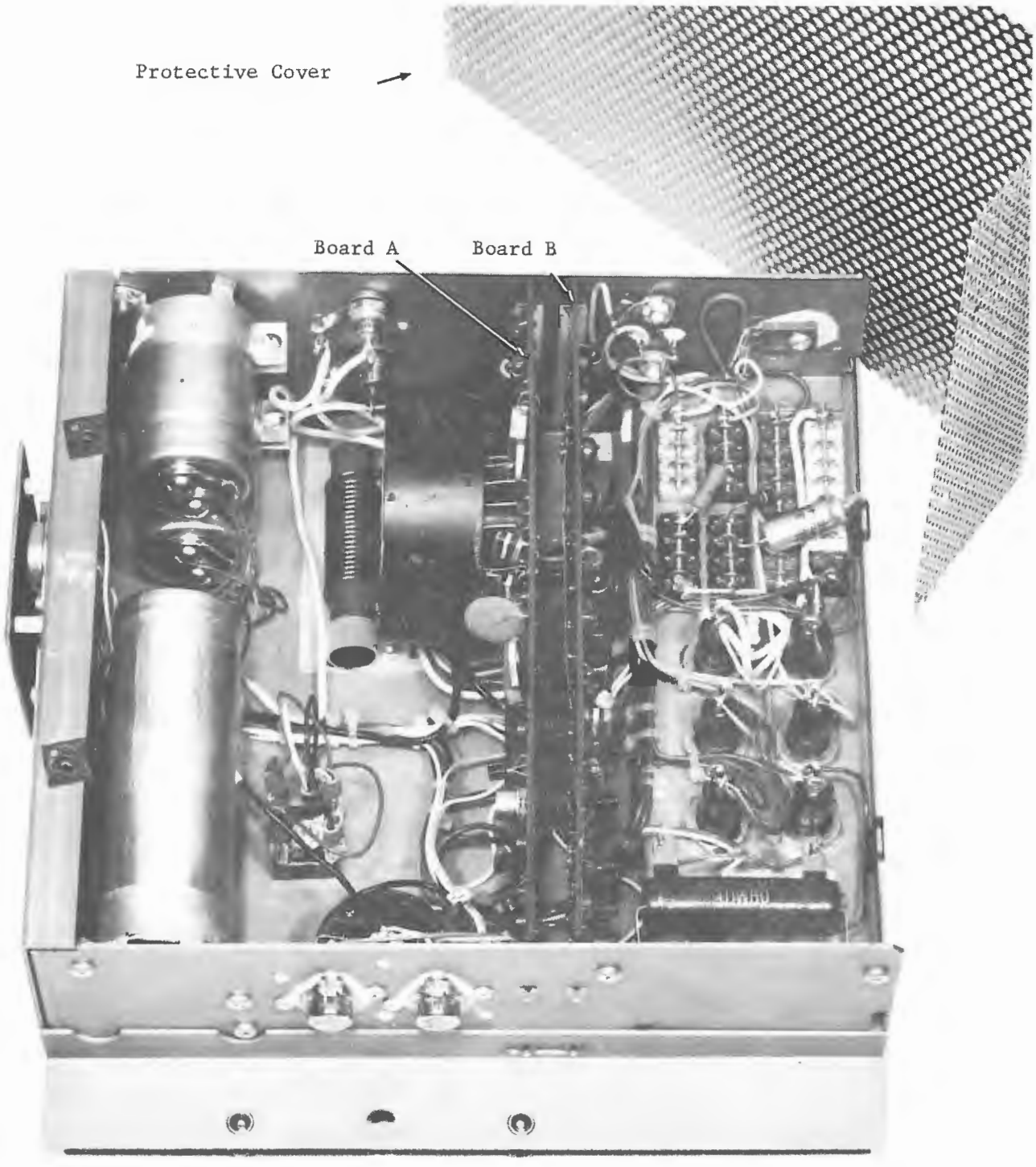


Figure 5-14. Internal View Power Supply

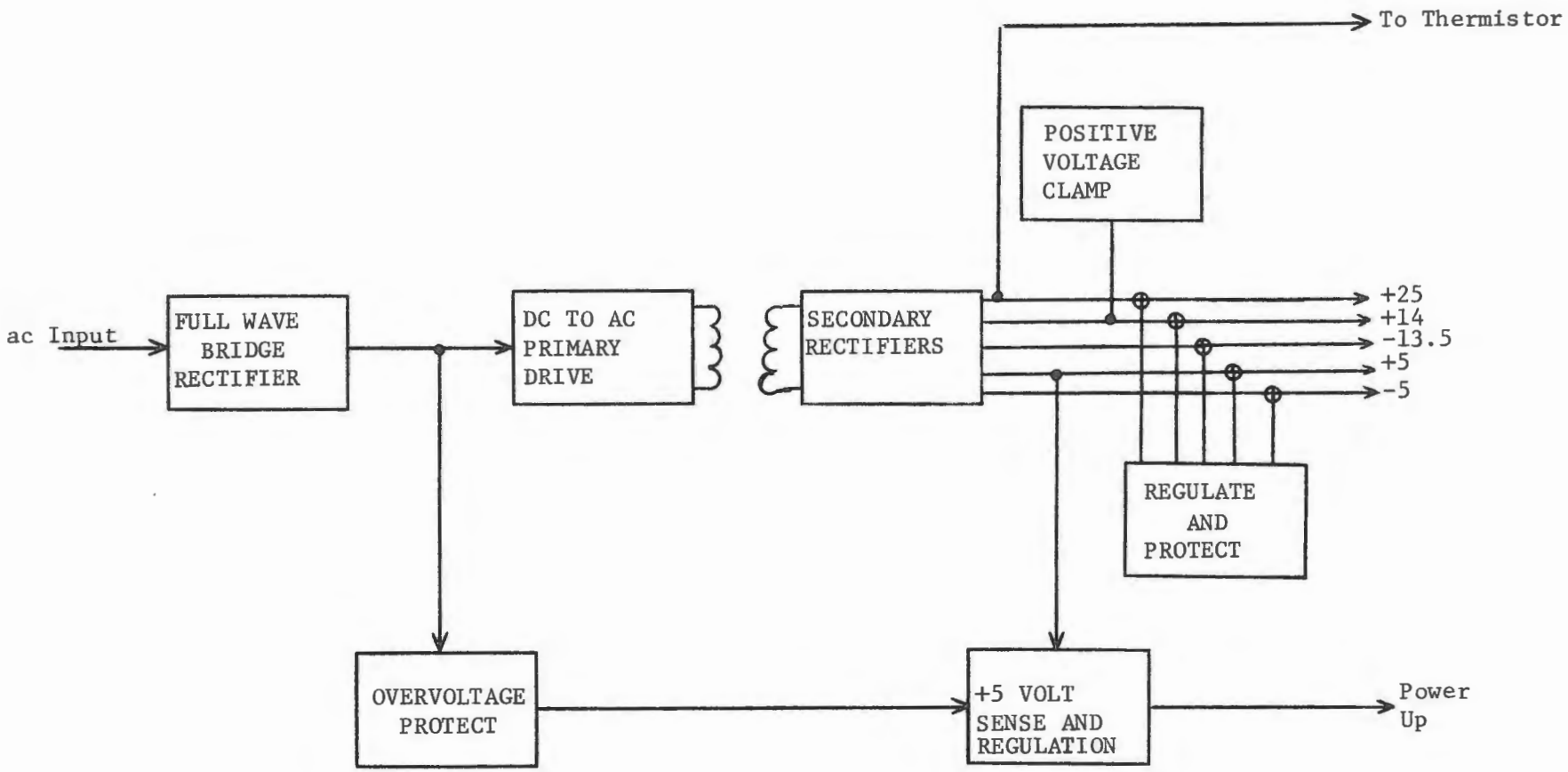


Figure 5-15. Simplified Block Diagram Power Supply

5.6.2 Operation

The Power Supply input is 115 VAC which feeds a full wave bridge rectifier. The rectified output is approximately 140 volts DC, measured at the positive side of C1, a 530 Mf capacitor. The rectified voltage is applied to the converter input circuitry (transistors Q2 and Q3) through diode D2 and associated circuitry. R32 provides dc bias to Q3 and causes Q2 and Q3 to oscillate. When oscillations start, the collector voltage of Q3 is reduced, which results in applying half of the input voltage (C2 and C3) to transformer T3 at the winding between pins 1 and 2. The polarity of the winding between pins 1 and 2 induces a voltage in the winding between pins 3 and 4. Pin 4 is the positive end and 3 the negative end. Transformer T4 winding from pins 1 and 2 is, for all practical purposes, parallel with T3 pins 3 and 4, therefore a voltage will be present across the T4 winding. The other two windings on T4 (pins 3 to 4 and 5 to 6) control the oscillation of Q2 and Q3. When Q3 is on, there is a V_{Be} drop (0.7V) and diode (D32) drop (0.7V), resulting in about 1.4 volts at the T4 winding between pins 3 and 4. Transformer T4 has a 1:1 turns ratio. The presence of DC voltage causes saturation of the transformer core which results in turning Q3 off. When oscillating, a 60 microsecond squarewave can be seen on an oscilloscope. The diodes at the secondary of T3 perform rectification and the system DC voltage is presented to the output, subject to regulation, over voltage protection, and the power up cycling provision.

5.6.3 Regulation

The windings across pins 10 and 12 on T3, produce a potential of 10 volts (pin 11 is chassis ground so the windings across pin 10 and 11 or 11 and 12 have a 5 volt potential across them). Diodes D6 and D60 rectify the positive voltage. There is a voltage drop through coil L6 which results in a voltage of close to +5 volts. The +5 volts is then routed to the 5 volt sense circuit and compared to a zener diode. When the +5 is normal (actually +5.2), D61, the zener diode, clamps to +5.2 volts and the comparison voltage enables the oscillation of Q61 and Q62 which results in a sine wave oscillation in transformer T2. The oscillation frequency is about 6 MHz. The oscillation in T2 is applied to the regulator circuitry and switches Q01 and Q1. The regulator serves two purposes: first, if the AC input voltage becomes higher than normal, T1 will sense it and cause switches Q01 and Q1 to turn on, thereby preventing the

overload from causing damage. Also, if +5 is not present, the fault is detected and again Q01 and Q1 protect the input circuitry. The output regulators are of the series type. The -13.5V and -5V are the simplest because there is only low power involved. Diode D81 clamps the +14 volt output and diode D71 performs the zener regulation for the -5 volt output. The +25V and +14V regulation is more complex. The +25 is regulated by a comparison involving diode D41. The +25 volts must track with temperature because the memory is sensitive to voltage changes. This tracking is accomplished by thermistor T in parallel with R43. Note that the thermistor is physically located on the memory stack. The +14 volt regulator utilizes Q51 and Q52 which compare the +14, the setting R51, R54, and R52 (R54 is a variable resistor). Q53 and Q54 are drivers driving the base of Q5, Q55 and Q56.

Overvoltage protection is accomplished with components R503, zener diode D51, and silicon controlled rectifier D52. Any voltage rising above the zener voltage will result in the silicon controlled rectifier (SCR) D52 shorting out the output of the +14 volt regulator.

The power up feature provides that the +5 volts must be present prior to the +14 volts on either power up or down so that the memory is never accidentally erased. Also, the design includes elimination of the +14 and +25 voltages if the +5 volts is not present. This is accomplished at transistor Q64. If the +5 volts is not present in the sense circuit, Q64 will pull down the +25 volts sense at the junction of R48 and R49, thus causing a loss of the +25V supply. Since the circuit for the +14 volt regulation utilizes the +25 volts, it also shuts down.

5.6.4 Typical Checks

When testing a power supply chassis, always use an isolation transformer and ground the negative side of the input bridge. As a first test, short the base of transistors Q01 and Q1 to the emitter. Under this condition the whole supply will act as a DC to DC converter, clearly indicating operational transformers, diodes, capacitors, and wiring of outputs. If this first test is successful, remove the shorts from transistor Q01 and Q1. Next, measure the +5 volts which will actually look like +5.2. If the power supply does not regulate at all, check the lead on both sides of J2-4. Problems in the D61, R62 and Q61 circuit can also cause no regulation. The base voltage on Q61

must be negative. Another power supply failure occurs if Q2 or Q3 become shorted to the chassis. As an added note, the supply generates much heat within the chassis; therefore, a warm component does not necessarily indicate the area of possible failure.

Some voltages and wave forms to observe are: the input voltage at the plus side of C1 is about 140 volts; voltage at cathode of D2 when regulating is between 280 and 300 volts; at fuse F4 the voltage is about +30 volts; at fuse F5 about +20 volts; at fuse F8 about -21 volts; at fuse F6 (at junction of L6) about +5. 5 volts; and at fuse F7 about -6 volts. When making ac measurements on the step down side of T3, note a voltage difference created by the double rectification of T3 winding between pins 10 and 12. This is due to a current unbalance which causes a voltage drop in the winding itself. The same is true of the winding T3 at pins 5 and 9.

5. 7 LINE LOCK OSCILLATOR

The Line Lock Oscillator is located on a two-inch by eight-inch circuit board which is mounted to the TPU frame adjacent to the power supply. The Oscillator, as illustrated in Figure 5-16, is crystal controlled and operates at a 12. 6 MHz frequency. When power is applied to the circuit, the resulting crystal vibration at 12. 6 MHz provides a voltage at the input of M1B. The output of M1B is fed back to M1A through C1. R1 and R2 provide a degree of linearity to the operation of the circuit. The oscillator output is buffered at M1C and fed out of the in-line pack at pin 3. Capacitor C2 performs a decoupling of the 5V line.

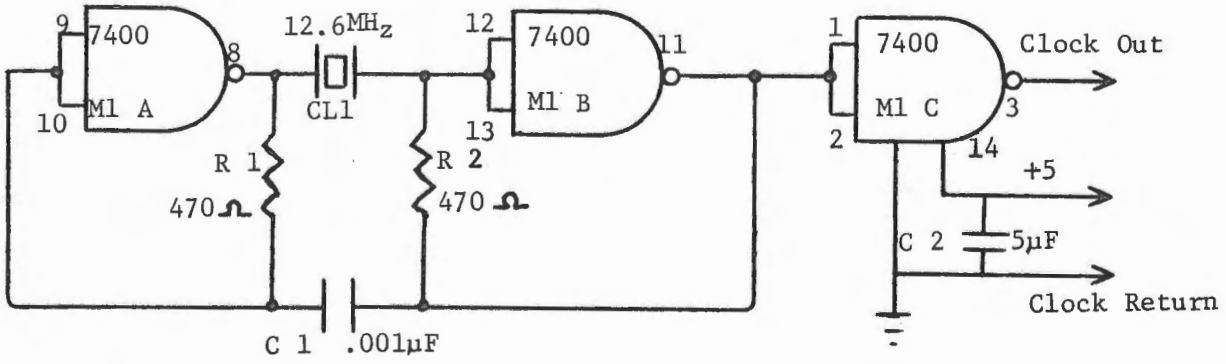


Figure 5-16. Line Lock Oscillator Schematic

CHAPTER VI

INPUT/OUTPUT INTERFACE CONTROL

6.1 INPUT/OUTPUT SYSTEM

The SPD 10/20 I/O system is composed of a functional group of interface electronic packages called I/O Controllers. The description of what happens on the Terminal side of the interface (from the I/O Bus into the computer circuits) is discussed in some detail in Chapter III, and at greater length in Chapter IV. The Programmers' Reference Manual, Section 7, further explains I/O interrupt handling and provides a functional description of I/O controller commands pertinent to the programmer. This chapter provides theory of operation for the various peripheral interface controllers. The discussion covers the keyboard unit and the following controllers: keyboard, asynchronous, synchronous, split screen and boot.

6.2 KEYBOARD

Operator interface with the SPD 10/20 data terminal is via a 76-key keyboard. The Keyboard is a vendor purchased item which is factory installed in the INCOTERM housing. In operation, the keys are individually ASCII encoded by the use of a core matrix at the keyboard. Figure 6-1 provides the encoding chart for keyboard 1090 - Rev. C, which is the one described. Stated simply, when a key is depressed, a properly routed current path is enabled from +5 volts to ground. Protection against two key rollover is provided by disabling the strobe if two keys are simultaneously depressed. Figure 6-2 is

CODE CHART, 1090-C KEYBOARD

$b_4 b_3 b_2 b_1$ \ b_7 b_6 b_5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0			Space 9	0 10	@ 24	P 23	Mode 67	67
0 0 0 1	58	Erase Line 58	⧖ 13	1 1	A 27	Q 14	68	68
0 0 1 0	55	Erase Scrn 55	⌐ 2	2 2	B 44	R 17	69	69
0 0 1 1	53	Ins. Line 53	# 3	3 3	C 42	S 28	70	70
0 1 0 0	56	Ins. Char 56	$ 4	4 4	D 29	T 18	71	71
0 1 0 1			% 5	5 5	E 16	U 20	72	72
0 1 1 0			& 6	6 6	F 30	V 43	73	73
0 1 1 1	26	Tab 26	’ 7	7 7	G 31	W 15	74	74
1 0 0 0	62	← 62	(8	8 8	H 32	X 41	75	75
1 0 0 1			) 9	9 9	I 21	Y 19	76	76
1 0 1 0			* 37	: 37	J 33	Z 40	↑ 60	60
1 0 1 1			+ 36	; 36	K 34	◀ 38	↓ 59	59
1 1 0 0	64	Line Ret 64	, 47	< 41	L 35	| 25	Home 61	61
1 1 0 1	54	Del Line 54	- 11	= 11	M 46	▶ 52	Xmit 65	65
1 1 1 0	57	Del Char 57	. 48	> 48	N 45		Print 66	66
1 1 1 1			/ 49	? 49	O 22	— 12	→ 63	63

Figure 6-1. Code Chart, 1090-C Keyboard

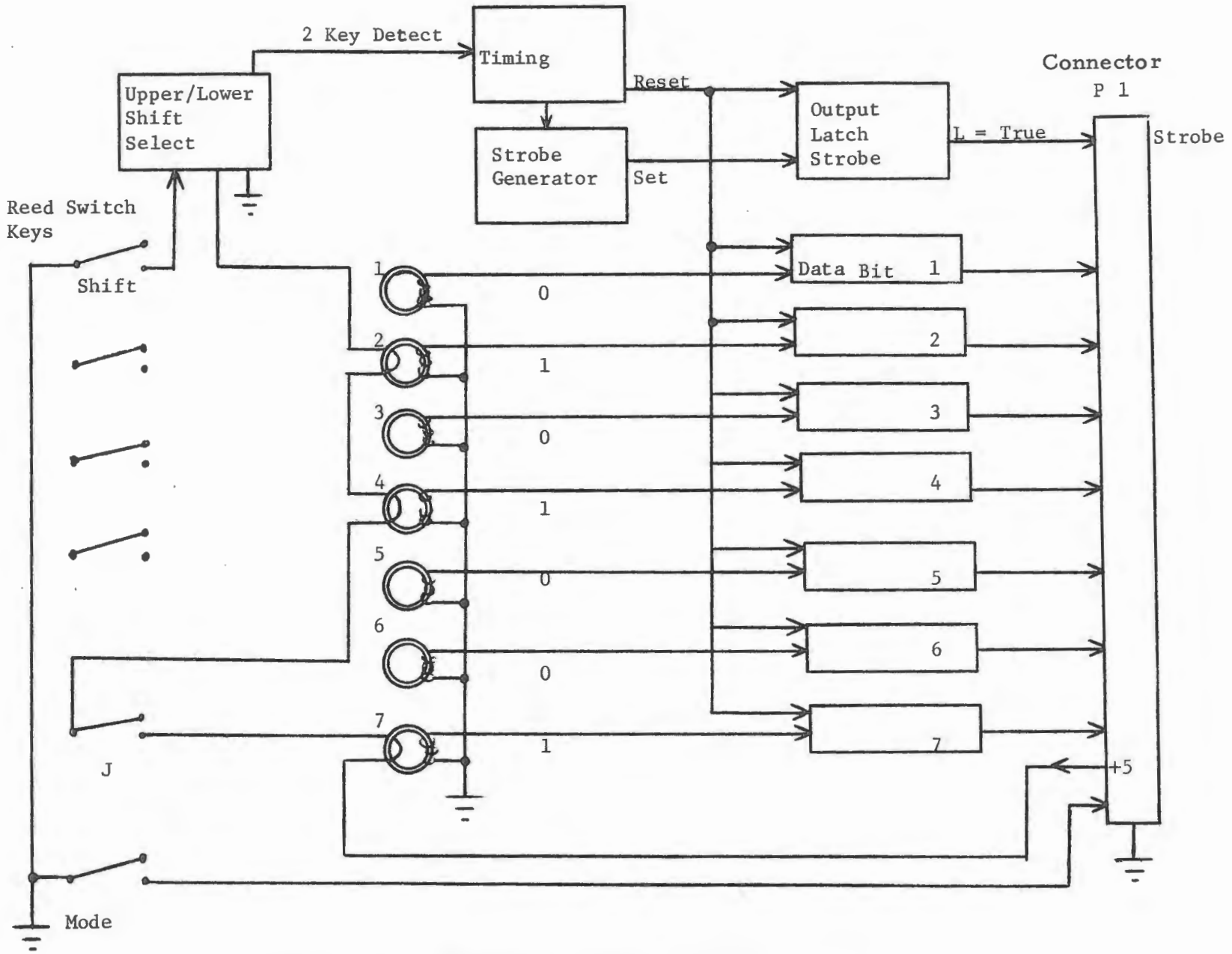


Figure 6-2. Simplified Keyboard Block Diagram Current Path Illustrated for J Key

a simplified diagram which is illustrated with core windings for a J key, the resulting code is:

BIT	1	2	3	4	5	6	7
J Code	0	1	0	1	0	0	1

In operation, when a valid key is depressed, the core matrix selected data code is entered into the output data register which is composed of 6 SN7402 quadruple 2-input positive nor gates N1 through N6 respectively. (Part of N6 is used for the strobe latch.) After data is entered, the strobe output is delayed by between 0.5 and 2 microseconds before it goes true (low). If, during this time or after it goes true, a second key is depressed, the strobe goes false until one of the two keys is released. The last one to be released is the key for which the data code will correspond. Optional MODE key operation is provided via a resistor change which can easily be implemented in the field. Under one condition the mode key when activated is provided directly to the output as a unique line. The other condition provides for encoding the line through the normal matrix and output registers.

The keyboard lamps, although physically located on the keyboard housing, are not a functional part of the keyboard electronic package. The lamps are installed at the INCOTERM manufacturing facility and are a function of TPU commands processed through the keyboard controller. The wiring to the keyboard is split at the keyboard end to provide for both the P1 connection and lamp connection. The following table lists the connections at the Keyboard.

Table 6-1. Keyboard Connectors

FROM TPU		Keyboard	Cinch Connector
		Pin 1	LSB Bit 1
		2	2
		3	3
		4	4
		5	5
		6	6
		7	MSB 7
		8	MODE
	MOLEX LAMP CONN.	9	STROBE
Pin 1	right most lamp, input bus LSB,	00 10	GND
2	2nd lamp from right	01 11	Conn. to 10
3	3rd lamp from right	02 12	+5 volts
4	4th lamp from right	03	

Table 6-1. Keyboard Connectors (Cont.)

FROM TPU			Keyboard	Cinch Connector
	Pin 5	5th lamp from right	04	
	6	6th lamp from right	05	
	7	7th lamp from right	06	
	8	8th lamp from right	MSB 07	
	9	N/C		

6.3 KEYBOARD CONTROLLER

6.3.1 Introduction

The Keyboard Controller is the interface between the TPU and the keyboard and all the circuitry is contained on one printed circuit board (see Figure 6-3). The controller accepts commands from the TPU, generates Interrupt Acknowledge signals, and provides data from the keyboard to the TPU. The logic for the Keyboard Controller is shown in drawing 001-03-01, sheets 2 and 3. Sheet 2 contains the control logic and sheet 3 contains the input/output data logic.

6.3.2 Input/Output Data

Inputs to the Keyboard Controller are shown on the left side of sheet 3. The controller address signal ADDXX is inverted by M12 (DSI00) and sent to pin 10 of M13 (ATCLAD), which is part of the circuit that determines the response of the controller to TPU Input/Output Commands. Type bits TYP 00 and TYP 01 determine the kind of I/O command: Control, Read, Write, or Test. The function bits (FUNC 02, FUNC 03, etc.) determine the function to be performed by a specific type command. For example, a Control I/O (CI/O) signal may designate a Mask or Unmask operation. The other input (pin 9) to M13 (ATCLAD) is connected to the phase 2 clock signal CPTO2N that is previously double inverted by M4 (IOICL1) and M4 (IOICL). When pins 9 and 10 are high, M13 (ATCLAD) is enabled (low) and its output is inverted by M1 (ATILAD) and is sent to pin 1 of M13 (ATGADCL). The other input of this gate (pin 2) is connected to the output of M6 (CIO) which is part of the Type Command decoding network (M5 and M6). The output of M6 (CIO) is high when a CI/O is decoded from the state of input signals TYP 00 and TYP 01. When both inputs of

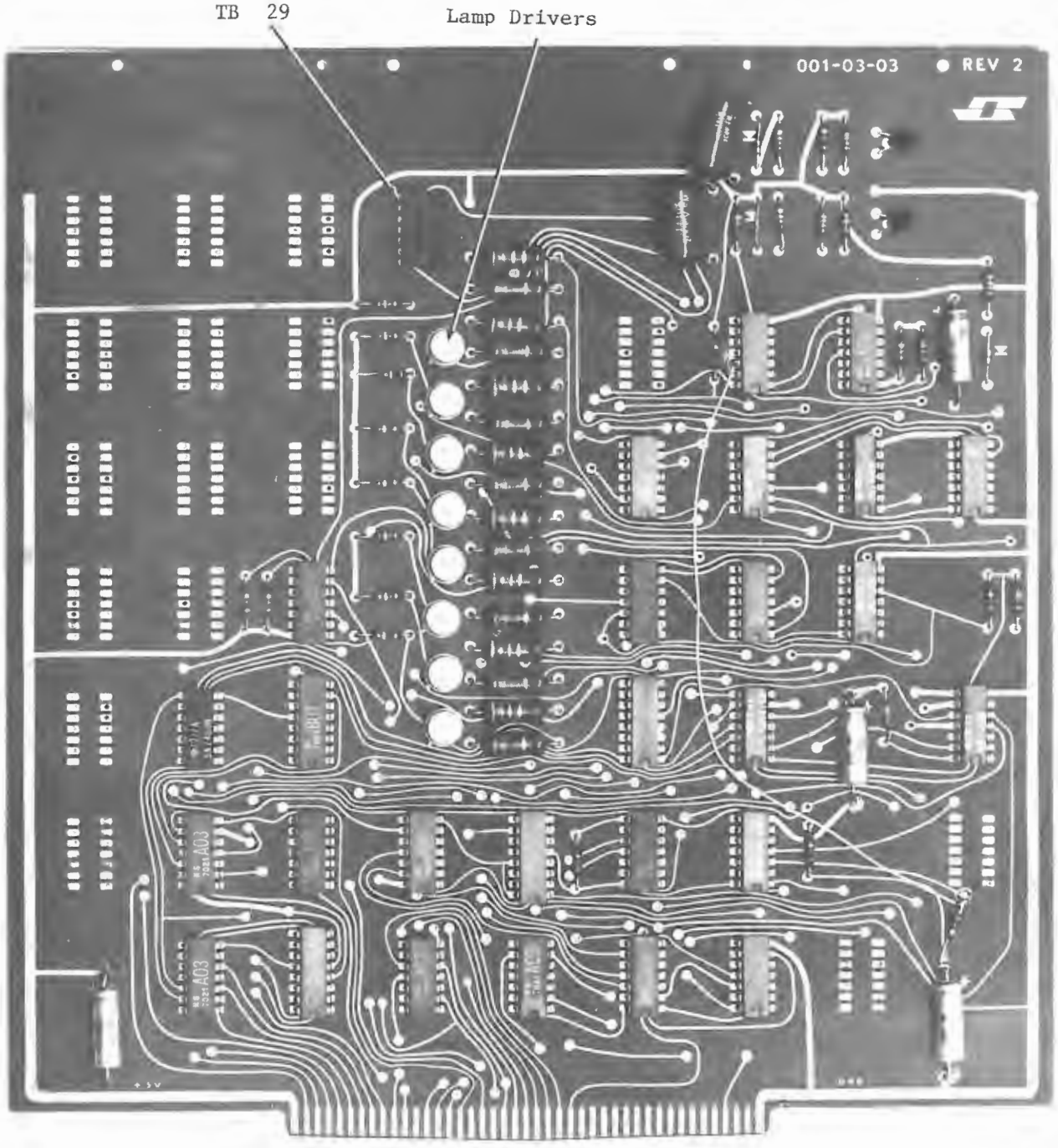


Figure 6-3. Keyboard Controller

M13 (ATGADCL) are high, it is enabled (low). This signal is enabled when a CI/O is decoded and the address (ADDXX) signal is low and a high phase 2 clock signal (CPT02N) is present. The output of this gate is inverted by M1 (ATIADCL) and sent to M13 (IRGFB) where it is anded with the inverted function bit FUNC 01 from sheet 2. This gate is enabled (low) when both inputs are high. Its output is inverted by M7 (IRICL) and M7 (IRICP) whose outputs clock M14 and M2, respectively. M14 and M2 are both 4-bit bistable latches whose outputs control the indicator lights on the keyboard. Inputs to the latches (M14 and M2) consist of 8-bits from the output bus (OTB 00 through OTB 07). Each bit is inverted by an M7 or M1 gate before application to the latch input. Each latch output is sent to one of eight identical lamp driver circuits shown at the right of sheet 3.

Operation of a typical lamp driver circuit is discussed; LT 00 for bit OTB 00 is used as the example.

The lamp driver circuit consists of a type 7405 inverter M18 (LT 00), drive transistor Q4 and a voltage divider network R22 and R30. This circuit is shown in Figure 6-4. Pin 52 is connected to the indicator which in turn is connected to +5V as shown in this illustration. Assume bit OTB 00 is low.

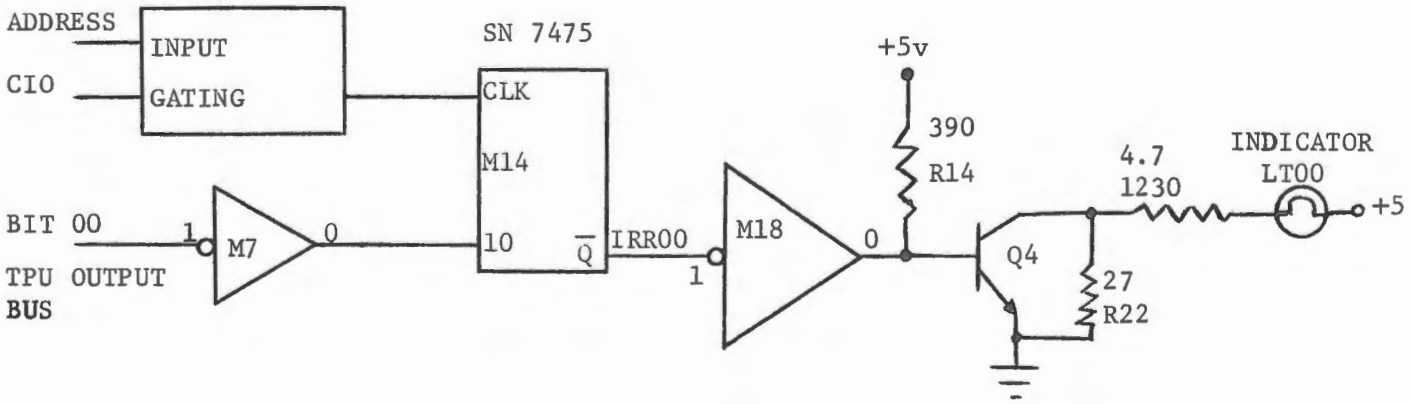


Figure 6-4. Typical Keyboard Lamp Driver Circuit (One Bit Shown)

After inversion, by M7, the input to D_1 of M14 is high. When clocked to the latch output, IRR 00 is low because only the $\overline{Q}$ output is used. This output is inverted by M18 and a high appears at the junction of the output of M18 and R14.

This high is at the collector of the output transistor of the inverter M18 which indicates that it is off. The +5V via R14 biases Q4 off and the indicator does not illuminate. Practically speaking, the light glows very slightly even with drive transistor Q_4 off because of the slight current flow in the R22/R30 divider network. This glow is used to check system power and to verify connection of the keyboard even if the input data does not request full illumination of the indicators. If bit OTB 00 is high, the output of M18 is low. Its output transistor is low which eliminates the bias from Q_4 and allows it to turn on. Current from the +5V at the indicator has a path to ground through the indicator, R30, and transistor Q4. The indicator is illuminated when the input bit OTB 00 is high. The indicators are under program control so it is possible for some of them to illuminate when power is applied. If the system is operating in a mode which does not require operative keyboard lights, the program commands all zeros on the output bus bits (OTB 00 through OTB 07) to the Keyboard Controller.

Flip flop M10 (MASK) controls the interrupt signal from the Keyboard Controller to the TPU via additional logic shown on sheet 2. If a CI/O Command is decoded and function bit 02 (FUN 02) is enabled (low), the next clock pulse via M1 (ATIADCL) sets M10 which represents a Mask Interrupt Command. In this state, an interrupt signal cannot be sent to the TPU. If function bit 03 (FUN 03) is enabled (low), flip flop M10 is reset which represents an Unmask Interrupt Command. In this state, an interrupt signal can be sent to the TPU. The Preset input (pin 7) of M10 is connected to the output of nand gate M24 (RESET). A low at pin 7 sets the flip flop to the one state ($\overline{Q} = 0$) regardless of the J-K inputs. This occurs when M24 is enabled; that is, when both inputs are high. M24 is enabled when a high phase 18 clock signal CPT18N is anded with a high RIORES signal from sheet 2 or a high RESET signal from the output of M4.

The gates (M3 and M9) for enabling the data from the keyboard to the Data Input Bus are shown on the lower center section of sheet 3. The 8-bit ASCII data from the keyboard is identified as KBDD 00 through KBDD 07. A gate is associated with each bit; for example, M3 (ACBDB 00) for bit KBDD 00. Gate M13 (KBOBO)enables the keyboard data gates. Normally, the gates are enabled by a low on pin 12 of M13 (KBOBO). The input signal ACGRIO is enabled on sheet 2 when the Keyboard Controller is in the Ready State and the

Address and Read I/O Command are present. The gates can be enabled by signal BOL 01 when in the Keyboard Boot state. This condition is described later in paragraph 6. 3. 3.

6. 3. 3 Control Logic

The Keyboard Controller control logic is shown on sheet 2. The logic at the top of the sheet is related to system operation in the Keyboard Boot mode. Gates M17 (BOL 00) and M16 (BOL 01) are interconnected to form a simple RS latch circuit. When the boot pushbutton switch on the keyboard is depressed, the M17/M16 latch is set by a low ENTBOOT signal to pin 1 of M17. The high output on pin 3 of M17 is inverted by M11 (BOOBUS) and is sent to the Control Board to the Boot State control logic which initiates Boot operation. The inputs to the other half of the latch, M16 (BOL 01), must all be high for the latch to be set. Pin 2 is high because it is always connected to +5V: it performs a power reset function to insure that the Keyboard Controller is not in the Boot mode when power comes up. Pin 1 is high because it is fed back from the output of M17. Pin 13 is kept high via M22 (BODKB), M26 (BOIKB) and M17 (BOLKB) as long as one input to M22 is low. All the inputs to M22 are high only if one of four keys are depressed: question mark, slash, seven or apostrophe. In this case, the low output of M22 (BODKB) is anded with a low keyboard strobe (KBST) at M26 (BOIKB). The high output of M26 is anded with a high phase 2 clock signal (IOICL) at M17 (BOLKB). The low output of M17 is sent to pin 13 of M16 which resets the latch and disables the Boot mode of operation.

The Acknowledge signal from the Keyboard Controller to the TPU is generated at the output of M11 (ACKKB). With respect to the Keyboard Controller, a Write I/O Command is normally typed data but the controller is not required to take the data as so defined. A W I/O is used by the controller as a Data I/O Command. Write I/O Commands to the Keyboard Controller are not acknowledged. This simplifies the Acknowledge circuitry. The keyboard Write I/O (KBGWIO) from sheet 3 is anded with the address signal DSI 00 from sheet 3 at gate M24 (ACGWIO). When both signals are high, an Acknowledge is generated via M22 (ACGIO) and M11 (ACKKB). Gate M16 (ACGTIO) acknowledges if the keyboard is present (connected and energized). Three signals are required to enable this gate: DSI 00 (high); KB PRESENT (low to

M12 (KBIKB)); and Test I/O signal TI 00 (high). Gate M16 (ACGRIO) acknowledges if the keyboard is ready to send data to the TPU. Three signals are required to enable this gate also: DSI 00 (high); READY (high); and Read I/O signal RI 00 (high). Gate M17 (ACGBOT) acknowledges only when the system is in the Boot mode and ready to send data. Two signals are required to enable this gate: DSI 00 (high); and BOL 00 (high) from the M17/M16 latch. A low output from any Acknowledge gate to M22 (ACGIO) produces an Acknowledge signal (ACK) from M11 (ACKKB).

The logic for decoding and generating interrupts to the TPU is shown in the center of sheet 2. M10 (INF 01) is a J-K flip flop that is connected in a specific way. Its J and K inputs are unused (both = 1) so that clock pulses at pin 1 toggle the flip flop. Pin 2, Preset input, is connected to the output of M21 (INGST): when pin 2 is low, the flip flop is preset to the one state (Q = 1). Pin 3, Clear input, is connected to the output of M20 (RIORES): when pin 3 is low, the flip flop is cleared to the zero state (Q = 0). M10 (INF 01) is initially set via M21 (INGST) when the keyboard strobe (KBST) comes true, provided the other conditioning signals to M21 are true. The outputs of M10 condition the J and K inputs of M15 (READY) so that the next IOICL clock pulse sets the Ready flip flop M15. The high Q output (pin 15) of M15 is anded with the high MASK* signal from sheet 3 (which represents the Unmasked state) at M21 (MAGRY). The enabled (low) output of M21 is inverted by M24 and is sent to the D-input of flip flop M19 (KBINT). The INTSELIN signal is inverted by M18 (INTSEL) and is used to clock M19. The low output ($\overline{Q}$) of M19 is double inverted by M24 and M18 and leaves via pin 30 as the Interrupt signal to the TPU. Gate M23 (INTFG) enables M24 by holding pin 2 high because pin 10 of M23 is connected to the $\overline{Q}$ output of M15. As long as M15 is set, $\overline{Q}$ (pin 14) is low and M23 is disabled (output is high). When M15 is cleared, M19 is also cleared and the Interrupt signal is disabled. M15 can also be set to the zero state if M10 is cleared via the reset signal REIET to M20 (RIORES) or via signals from M23 (RIOCG) and M12 (RIOIG). This action also disables the Interrupt signal.

Generating an interrupt to the TPU indicates that a character is ready. The character is taken in and the sequence ends unless another key is depressed or it is desired to repeat the same character. There are two ways to implement a key repeat function. One way is for the TPU to send along a

Write I/O Command which is interpreted as a Control I/O Command. The keyboard acknowledges the W I/O and the controller generates an interrupt to the TPU if the strobe (KBST) is still present and the same key is still held down. This function is performed by M21 (INGST) and M10 (INF 01). The other way to implement a key repeat function is via the circuitry represented by the Repeat Key Enable flip flop M19 (RPKEN), one-shot circuit M25 and associated gates (M20, M23, and M28). Enabling Function Bit FUNC 00 indicates that the TPU considers the situation to be a valid key repeat condition. FUNC 00 is inverted by M8 and is applied (high) to the D-input of M19 (RPKEN). Clock signal ATIADCL sets M19. The high Q-output of M19 is anded with an inverted (high) true keyboard strobe signal (KBIST) at M28 (RPKEYS). The enabled (low) output of M28 is sent to the Preset input (pin 10) of M19 which holds M19 in the one state (Q = 1), as long as it is present. If the keyboard strobe goes false, M19 is cleared by KBIST at the Clear input (pin 13). A low IDICL clock signal is anded with the low $\overline{Q}$ output of M19 at M20 (RKGCL). The high output from M20 is anded with a high REIDL signal and the pulse output from the one-shot M25. In effect, the pulses from the one-shot clock M10 (INF 01) via M23 (RPGEN) and M17 (INTGCL) at a rate determined by the pulse duration. Each time M10 is set, an Interrupt is generated to the TPU.

As an option, the Terminal can be equipped with a device that generates an audible tone to alert the operator to an error condition. The device is mounted on the chassis and is driven by the circuitry shown at the bottom of sheet 2. It is identified as the BUZZ circuit but the device actually generates a pleasing tone. The BUZZ output is taken from pin 79 and is controlled by the logic shown to the left of drive transistor Q_3. The BUZZ gate M26 is enabled by anding low signals from M8 (BUZZI) and M11 (ATGWIO). The inputs to M11 represent a W I/O present (KBGW I/O) and the presence of the Keyboard Controller address anded with a phase 2 clock signal: the resulting signal is inverted and sent to M11 as ATILAD. The actual BUZZ circuit input signal is MAISK which is the inverted FUNC 02 signal from sheet 3.

6.4 ASYNCHRONOUS CONTROLLER

6.4.1 General

The Asynchronous Controller (see Figure 6-5) normally connects to an asynchronous data set and provides the complete interface between it and

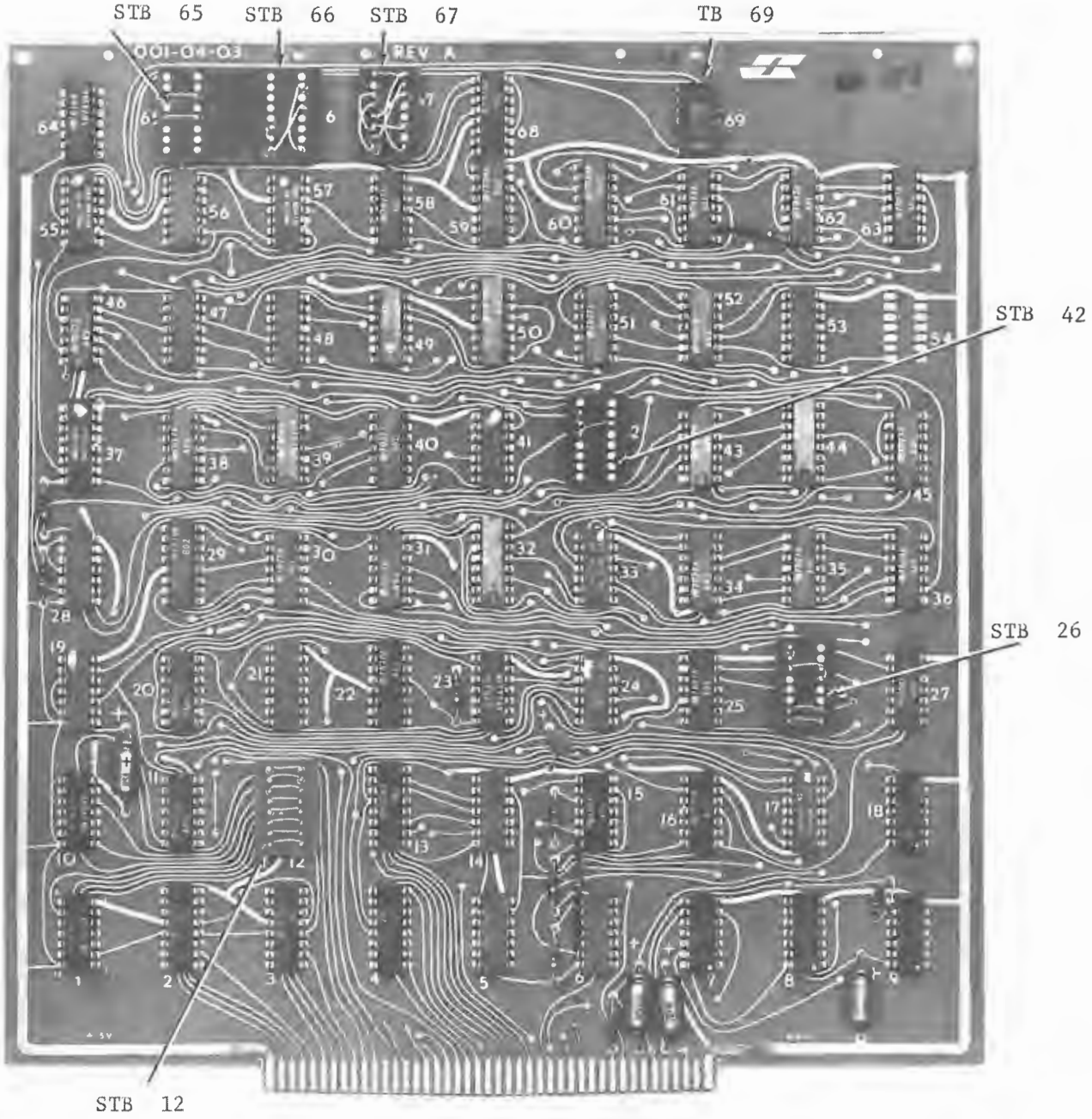


Figure 6-5. Asynchronous Controller

the TPU. The controller receives serial data from the asynchronous data set, and converts it to parallel data which, in turn, feeds into the Terminal Processor Unit. Likewise, the asynchronous circuitry takes parallel data from the Terminal Processor Unit and transmits it serially to the data set. Theory of operation is referred to schematic 001-04-01, sheets 2 through 5. Figure 6-6, a simplified block diagram, can be followed as the description of each schematic is generalized. Table 6-2 describes the option blocks for this controller.

Sheet 2 consists primarily of the register section. The bus out lines OTB 00 through OTB 07 represent 8-bit parallel data from the TPU. They are sent to the Parallel Input Register (M2 and M3). The next register, M5 and M14, is the Serial Register (SR). When operating in the WRITE mode, input data is entered serially and shifted out in parallel to the Parallel Output Register (M4 and M13). The parallel output data in turn goes through a word length option block (STB12) and into Gates M1 and M10 which are strobed into the Bus In lines (INB 00 through INB 07) to the processor. This circuitry also provides parity checking for the receive mode, parity generation for the WRITE mode, and signals to a multiplexer which indicate whether the particular unit has data.

Sheet 3 consists basically of logic which performs the control decoding. The function code is a four condition, 2-bit control signal and the type code is 2-bit, two condition control signal. The control decoding is the major function of this board, but in conjunction with it, system clocks utilized for asynchronous control are shown on the schematic. The type decode provides the Read I/O, Write I/O, Test I/O and Control I/O outputs. The Type I/O's are anded with the decoded function signals to produce the different T I/O's. The T I/O's are all located on Sheet 3 and are functionally grouped at AND gates M23. The C I/O Write (C IO 2) and C I/O Read (C IO 3) signals place the controller either in the Write or the Read mode.

Sheet 4 contains the controller timing circuits. The high speed system clock TURT4 provides the basic time reference which is divided down to provide an equivalent data set speed. The Data Clock generator circuitry is composed of digital differentials of the actual data set clock itself. The six flip flops, M50 (2), M59 (2) and M68 (2), operate as a bit counter of the

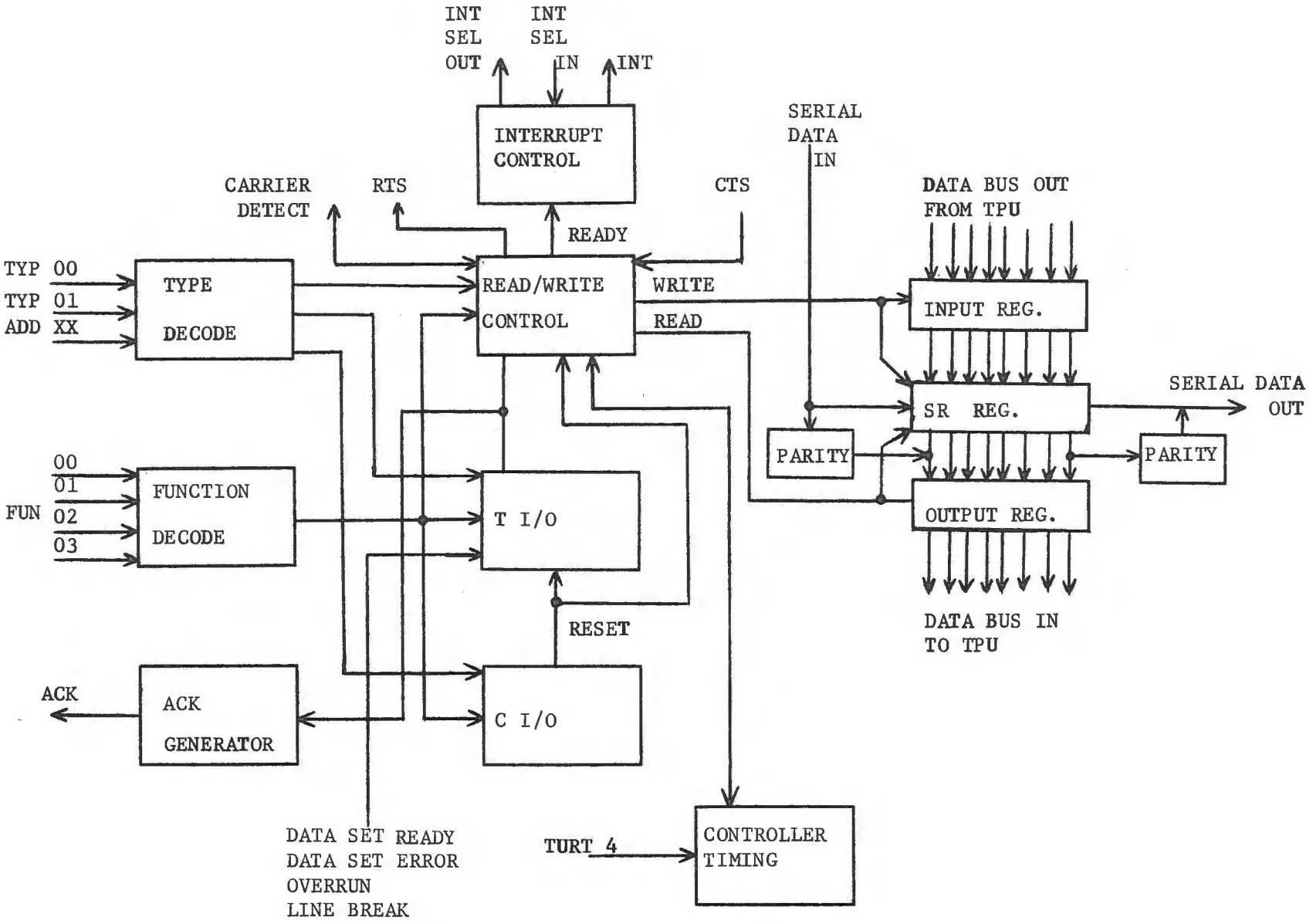


Figure 6-6. Block Diagram Asynchronous Controller

Table 6-2. Asynchronous Controller Option Blocks

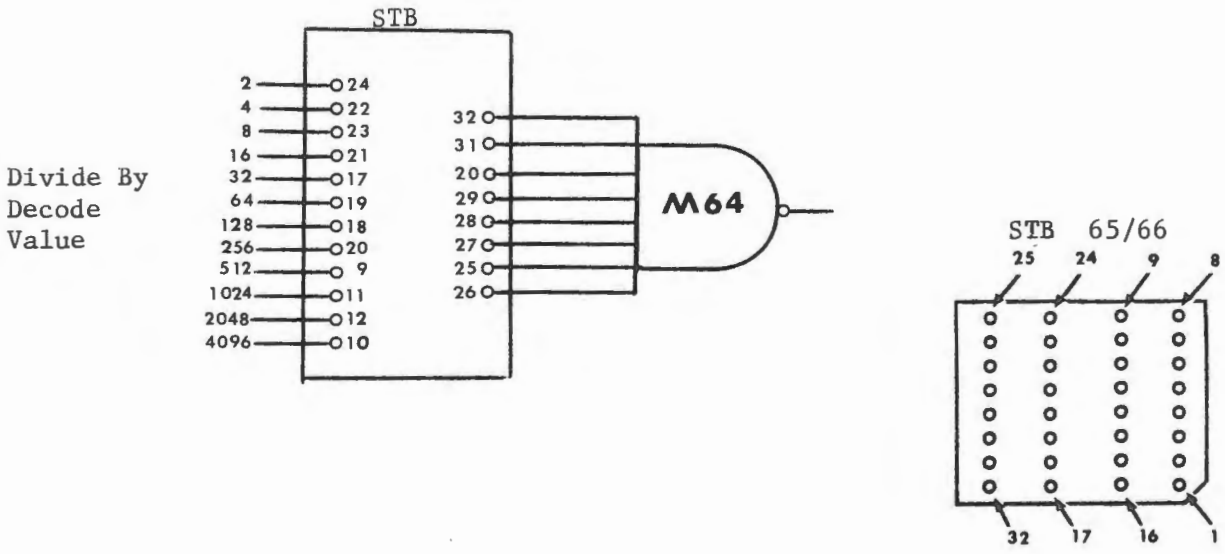
STB 12	for	8 Data Bits	for	7 Data Bits
		1 to 16		1 to 15
		2 to 15		2 to 14
		3 to 14		3 to 13
		4 to 13		4 to 9
		5 to 12		8 to 10
		6 to 11		7 to 11
		7 to 10		6 to 12
		8 to 9		
	for	6 Data Bits	for	5 Data Bits
		1 to 14		1 to 13
		2 to 13		2 to 9
		3 to 9		3 to 10
		4 to 10		4 to 11
		8 to 11		8 to 12
		7 to 12		
STB 26	for	Standard RS232 and Printer Operation	for	Multiplexer Operation
		1 to 16		1 to 16
		2 to 15		2 to 15
		5 to 6		5 to 6
		6 to 11		6 to 11
		9 to 10		8 to 9
	for	Direct Connect to Tele Type (using turn around cable)		
		1 to 3		
		14 to 15		
		5 to 6		
		6 to 11		
		9 to 10		

Table 6-2. Asynchronous Controller Option Blocks (Cont.)

STB 42	for	Stand RS232 Asynchronous Modem and Printer and Teletype Direct Connect	for	Synchronous Modem
		6 to 12		6 to 12
		7 to 8		5 to 8
		10 to 11		3 to 14
				10 to 11
	for	Multiplexer tied to Asynchronous Modem	for	Multiplexer tied to Synchronous Modem
		6 to 12		
		7 to 8		2 to 16
		14 to 11		3 to 13
		2 to 16		4 to 11
				5 to 8

STB 65, 66	for	Parity Check and Gen	
	1.	for No Parity Check	1 to 13
	2.	for Transparent Parity	1 to 2
	3.	for Even Parity Check	1 to 7
	4.	for Odd Parity Check	1 to 6
	5.	for No Parity Gen	16 to 13
	6.	for Transparent Parity Gen	16 to 3
	7.	for Even Parity Gen	16 to 5
	8.	for Odd Parity Gen	16 to 4
	for	External or Internal Clock	
	1.	for Internal Clock to be Used with Async Modems	15 to 14
	2.	for External Clock to be Used with Sync Modems	15 to 8

Table 6-2. Asynchronous Controller Option Blocks (Cont.)



STB 65, 66 Directions: for Specific BAUD Rate

1. Determine duration of one bit in microseconds (μsec).
2. Divide duration result by 2.
3. Multiply result of division by 0.63.
4. Take result of division and match as closely as possibly the divide by decode values.

Example: for 1200 BAUD

1. $\frac{10^6}{1.2 \times 10^3} = 0.83333 \times 10^3$ μs = 833.33 μsec.
2. 833.33/2 = 416.67 μs.
3. 416.67 x 0.63 = 262.49.
4. The closest divide-by decode value to 262.49 is:

   256 + 4 +2 = 262.

   Note % error = $\frac{262.49 - 262}{262.49} = \frac{.49}{262.49} \cong 0.2\%$ error.

Thus the pin assignment for divide by decode value 256 is 20.
the pin assignment for divide by decode value 4 is 22.
the pin assignment for divide by decode value 2 is 24.

Table 6-2. Asynchronous Controller Option Blocks (Cont.)

Now wire from Pin 20 to any one of the and inputs of 7430, M64. Repeat wiring of Pin 22 to another input for Pin 22 and again for Pin 24. Leave all other inputs open. For example: Tie pin 20 to 29, tie pin 22 to 27, tie pin 24 to 25. These three wires will establish a 1200 BAUD rate.

STB 67 for 11 Bit Data - 1 Start Bit
8 Data Bits
2 Stop Bits

1 to 9
2 to 8
3 to 10
6 to 13
7 to 15
11 to 14
12 to 16

for 10 Bit Data - 1 Start Bit
8 Data Bits
1 Stop Bit

1 to 8
8 to 9
3 to 14
14 to 11
6 to 13
7 to 15
12 to 16

for 8 Bit Data - 1 Start Bit
5 Data Bits
2 Stop Bits

1 to 12
12 to 8
3 to 6
4 to 14
7 to 13

for 8 Bit Data - 1 Start Bit
6 Data Bits
1 Stop Bit

1 to 12
12 to 8
3 to 6
4 to 14
5 to 16
6 to 15
7 to 13

Johnson type. The remaining circuitry on this schematic consists of all the input and output lines to and from the data set.

Sheet 5 contains the Read/Write control logic. The Interrupt signal only occurs when the controllers is receiving or sending data. An example of its significance is when, in the Read mode, a character is on the parallel input bus and as soon as the R I/O is received, the asynchronous controller sends the data. In the Write mode, the interrupt indicates the acceptance of the last W I/O character, and the controller is ready to receive the next W I/O character.

The Asynchronous Controller can interface with asynchronous type data sets, the SPD-P Printer, and any type of asynchronous data. The Asynchronous Controller data handling can be in five bit, six bit, seven bit, or eight bit formats; in other words, the message option block STB67 can be lengthened or shortened at the bit counter. Typical data blocks are: five bit data with one start bit and two stop bits; six bit data with one start bit and one or two stop bits; seven bit data with one start bit and one or two stop bits; or eight bit data with one start bit and one or two stop bits.

The Asynchronous Controller can also interface with synchronous data sets. To accomplish this, it must receive a clock from the data set. This requirement is accomplished in the Write mode by using the data set clock. In other words, the synchronous data set provides the transmitter clock, which is used to transmit the data, and synchronize the system. In the Read mode, only receive data comes in. The first data bit will be a zero followed by data bits and ending with one or two stop bits. The only thing required in this case is to set the divide-by clock accuracy so that it is within a tolerance of less than two percent compared to the clock of the data set. As long as it is that accurate, the synchronous data will operate as if it were asynchronous data with no need for synchronization. The various Baud rates are selected at option blocks STB 65 and STB 66. Table 6-2 illustrates the jumper connections and resulting Baud rate selection. Initially, SPD 10/20 Terminals are operating with 8-bit data, one start bit and two stop bits, which is the most common configuration. When using higher Baud rates, the bit rate is slower and only one stop bit is used. For the remainder of this discussion, assume the standard length word to be 8-bit data, one start bit and two stop bits.

The Asynchronous Controller operates in only two states: the Write mode or the Receive mode. The controller is placed into the Write mode by the TPU. When the Write mode ends, either by a reset or by normal turn-around, by definition the controller goes into the Read mode. This action insures that the controller is always ready to receive, if it is not writing.

The following paragraphs contain a general discussion of the major functional units and operating modes associated with the Asynchronous Controller.

6.4.2 Timing Circuits

The timing circuitry of the controller (see sheet 4) provides a count down of a basic clock signal to provide an equivalent data set clock whose rate is selected by a hard wired option. System clock signal TURT4 is counted down by the Divide-By Counter (M55, M56 and M57). The counter is composed of three 4-bit binary counters in a cascaded connection to provide 12 outputs. The outputs provide simultaneous divisions (2, 4, 8, 16, ··· 4096) that are connected to option blocks STB 65 and 66. The connection configuration of these option blocks provides the selected Baud rate. Directions for selecting the Baud rate are contained in Table 6-2. The option block outputs are anded at gate M64 (DCDI) which is sent to the inputs of flip flop M37 (DCK0). M37 is clocked by a function of TURT4 via gate M40 (STRCK). The output of flip flop M37 is effectively the data set clock and its rate is determined by the configuration of option blocks STB 65 and 66. This output passes through option block STB 66 where the selection of external clock or internal clock is made. The external clock is used with a synchronous modem and the internal clock is used with an asynchronous modem. The output of M37 is also sent to the logic shown in the upper right section of sheet 4 (M47, M48, M40, M49, etc.) where additional data clock signals are generated. These data clock signals (DC1, DC2, and DC3) are used in the control logic. The Bit Counter (M50, M59, M68) consists of six J-K flip flops connected as a Johnson Counter which requires a simple decoding network that can be altered by option block STB 67 to provide a variable length data character (8 to 11 bits). Refer to Table 6-2 for STB 67 wiring instructions. The Bit Counter is clocked by signal DC1*. It is enabled and disabled by signal BCT ENABLE/DISABLE from sheet 5 which simultaneously controls the CLEAR input of each flip flop. A low signal clears the flip flop.

6.4.3 Input/Output Commands

The Asynchronous Controller responds to several I/O Commands from the TPU which are categorized below.

Control I/O Commands (C I/O)

1. C I/O Reset - Clears all errors in the controllers and places it in the receive condition.
2. C I/O Write - Initiates the Write sequence and generates a Request to Send signal.
3. C I/O Read - Initiates the Read mode.
4. C I/O Data - Used only in the multiplex mode after a C I/O Write to indicate to the Multiplexer that the TPU has priority data to send.
5. C I/O Unmask - Allows the normal Read or Write interrupt signal to be sent to the TPU.
6. C I/O Mask - Inhibits interrupts from being sent to the TPU.

Test I/O Commands (T I/O)

1. T I/O Controller On-Line - Controller acknowledges if it is operational.
2. T I/O Data Set On-Line - Controller acknowledges if the data set is connected, turned on and the Ready signal is present.
3. T I/O Data Set Error - Tests for lack of carrier in Read mode; lost or intermittent carrier during the reading of a character; or loss of Clear to Send signal in the Write mode.
4. T I/O Overrun - Tests, during the Read mode, that the TPU has received a character before the next character is transferred to the Data Bus In lines.
5. T I/O Line Break - Tests for a Line Break in the Write mode. A Line Break is defined as the detection of a Start bit on the input line when the controller is sending a Stop bit.

Write I/O Commands (W I/O)

1. W I/O Write Data - Controller acknowledges if it is ready to receive a character for transmission.
2. W I/O Line Break - Causes the controller to place a continuous spacing signal on the output data line.

Read I/O Command (R I/O)

There is only one signal in this category: R I/O Read Data. This signal acknowledges that a character is available for transfer to the TPU.

6.4.4 Write Mode

In the Write mode, the TPU sends data to the Asynchronous Controller in parallel bit, serial character format. The controller converts this data to serial bit, serial character format and transmits it to the Data Set. A general discussion of the Write mode, from controller preparation to last character transmission, is presented in the following paragraphs.

The TPU sends the first character on the Bus Out lines along with a W I/O and ADDXX that are decoded by M21 and M38 (sheet 3). The decoded signal is sent to gate M24 (sheet 4) where it is anded with FUNC 00 and a signal from the Ready flip flop. The output of M24 (pin 12) is sent to M6 (sheet 3) which generates the Acknowledge signal (ACK) to the TPU. In this case, the output of M24 (pin 12) represents a W I/O Acknowledge but it also can represent a R I/O because both commands are decoded by the same circuitry and sent to M24. The output of M24 also generates the parallel input strobe (PAR IN STROBE) at gate M17 which puts the character on the Bus Out lines (OTB 00 through OTB 01) into the Input Register M2 and M3 (sheet 2). The Bit Counter (M50, M59 and M68) starts counting. It counts 0 through 10 for 11-bit data. Just prior to bit count 1, the data in the Input Register is strobed into the Serial Register (M5 and M15). During bit counts 1 through 10, the character is serially shifted out of the Serial Register. At bit count 8, the parity bit is added to the outgoing serialized character. The controller is set to the Ready state simultaneously with the transfer of the first character from the Input Register to the Serial Register. This indicates that the controller is ready for the next character from the TPU. If the controller is unmasked, it will generate an interrupt to the TPU via gate M34 (sheet 5). The TPU places the next character on the Bus Out lines and issues a W I/O and ADDXX which starts the sequence again. After the first character is sent by the TPU and acknowledged by the controller, the TPU issues a C I/O Read signal to initiate a turn-around. However, the controller just accepted a character so that a

character is in the Input Register and one is in the Serial Register. Therefore, there must be a delay of two character times to insure transmittal of the two characters in process before the turn-around is enabled. The logic shown on the top center section of sheet 3 provides this delay.

6.4.5 Read Mode

In the Read mode, the Asynchronous Controller receives data from the Data Set in a serial bit, serial character format. It converts the data to a parallel bit, serial character format and sends it to the TPU. A general discussion of the Read mode is presented in the following paragraphs.

Serial data from the Data Set enters the Asynchronous Controller via pin 66 which is the input to Line Receiver M9 (see sheet 4). The other Line Receivers (M7 and M8) detect other status signals from the Data Set to insure that it is operational. The serial data in (SDI) is sent to the input of flip flop M32. During the Write mode, M32 is held set by a signal from the Write flip flop (WRT F/F*). If the incoming data is valid, the first bit is a zero and represents the start bit of the first character. This condition is detected in the logic shown at the top left section of sheet 5. This logic generates the signal BCT ENABLE/DISABLE that enables the Bit Counter (M50, M59, M68) on sheet 4. Simultaneously, the Divide-By Counter (M55, M56, M57) is enabled and it results in the generation of data clock signal DC1* which clocks the Bit Counter. The Bit Counter counts for 8, 9, 10 or 11 bits, depending on data word length and the number of stop bits. The incoming data bits are sampled in the center of each bit to check for discrepancies. The character is shifted into the Serial Register by signal DC1*. When a complete character is in the Serial Register, it is shifted into the Output Register (M4 and M13) by the Parallel Output Strobe from sheet 2. Parity is checked as the data enters the Serial Register. When the character is shifted into the Output Register, the controller interrupt is turned on. If the controller is unmasked, the interrupt is sent to the TPU. The TPU responds by sending an R I/O and ADDXX. The controller sends an Acknowledge signal which resets the interrupt. At that time, the data is sent to the TPU. This is accomplished by the Parallel Input Strobe signal which enables gates M1 and M10 (sheet 2) to the Bus In lines (INB 00 through INB 07). When the next character is shifted from the Serial Register to the Output Register, the controller's Ready flip flop is set, and then reset by the correct response from the TPU.

6.4.6 Boot Mode

In the Boot mode, the Boot Controller sends a signal to the Asynchronous Controller to inhibit the Acknowledge signals from the Asynchronous Controller. The TPU is in the Boot mode and the Asynchronous Controller sends data to the Boot Controller with the Boot Controller issuing the control functions. The Asynchronous Controller receives a Data Received signal from the Boot Controller which indicates that the Boot Controller has received the Character Available signal from the Asynchronous Controller and sets the Ready flip flop.

The Asynchronous Controller sends three signals to the Boot Controller.

1. Character Available - Indicates that a character is available at the Asynchronous Controller.
2. Xmit Data - Indicates which mode the Asynchronous Controller is in (Read or Write).
3. Carrier Detected - Indicates whether or not the Carrier Detect is on.

6.5 SYNCHRONOUS CONTROLLER

6.5.1 General

The Synchronous Controller is used at higher Baud rates than those for asynchronous transmission. The present data rate of 2400 Baud (bits per second) can be increased because operation is based on an external clock source. At data rates of 2400 and below, normal telephone lines can be used; however, at speeds above 2400 Baud, direct lines are required. Physical circuitry is mounted upon a circuit board which conforms to the same dimensions as all other Input/Output controllers (see Figure 6-7). When system operation is Synchronous, half duplex, one circuit board is used and is generally located in I/O slot 2. If full duplex operation is desired, two Synchronous controllers must be used. The controller can interface with Type 201A and B Modems, standard RS 232 compatible devices, SPD-M Multiplexers or INCOTERM Boot Controllers.

6.5.2 Circuit Options

As illustrated in Figure 6-7, there are a number of locations on the circuit board where an individual customer requirement can be provided by installing option block headers. Option type and associated block include the following.

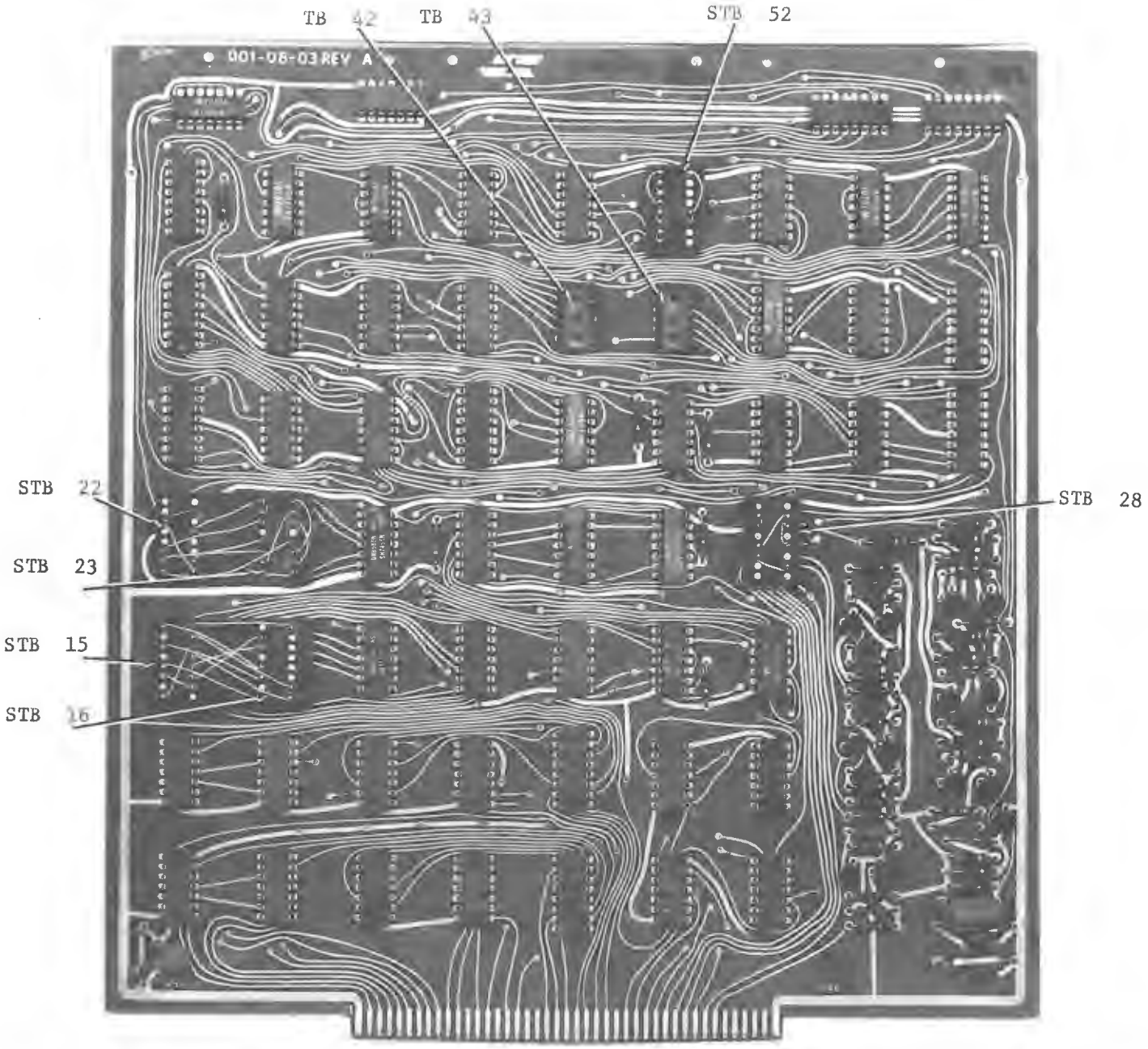


Figure 6-7. Synchronous Controller

16 pin Option Blocks

- STB 28 - Multiplexer/no multiplexer operation
  Data Set Ready
  Request to Send
  New Sync/no New Sync
- STB 52 - Parity/no Parity

32 pin Option Blocks

- STB 22/23 - World Length
  Multiplexer
  Sync Detect
  Transmit Parity
- STB 15/16 - Sync Codes
  Timing

Synchronous transmitted data must contain some format or pattern of synchronization. The SPD 10/20 Synchronous Controller precedes every data envelope with sync codes. The Controller can decode any 8-bit code with sync codes and can be optioned to determine how many consecutive sync codes have to be received before establishing the data transfer. In addition to the ability of optioning the sync codes, 6, 7 or 8 bit data can also be optioned; however, the actual data is transparent to the Controller. The data word option can be with or without parity, and parity can be odd or even.

6.5.3 TPU Control and Modem Interface

Programmed command signals for synchronous operation is somewhat similar to I/O commands previously described which include the Control (C I/O) I/O, Test (T I/O) I/O, Read (R I/O) I/O and Write (W I/O) I/O (see the Programmers' Reference Manual for a description of the coding functions).

The Modem interface conforms to the standard RS 232 specifications. Most Modems are compatible with RS 232, but some take advantage of unused lines to include signals specific to a certain type modem. The Synchronous Controller includes the option for a feature found on many new high speed modems called NEW SYNC. The New Sync feature allows the Controller to squelch a receiver, thereby eliminating line reflection or ringing which sometimes occurs when a device stops transmitting. This feature allows faster access to the line and eliminates the possibility of having the transmitted data be received with errors due to noise on the line. The Request-to-Send to modem can be hard-wired On at STB 28 or controlled by a programmed C I/O.

This option is useful when the configuration is point to point, in which case turn-around time is saved by not requiring the RTS to be set and reset. Another controller to modem signal is the Data Terminal Ready, which is a Voltage level that most modems require. The DSR can be optioned at STB 28.

6.5.4 Multiplexer Operation with Synchronous Controller

The basic difference between modem and Multiplexer operation is the Clear-To-Send (CTS) line. In the modem situation, the CTS is a voltage level which indicates a data transmit can be performed. When operating with a Multiplexer, the modem CTS is combined with the modem clock and thereby eliminates one interface wire.

The Multiplexer operation can include up to 16 Terminals and in this multiple transmission mode, the Multiplexer must discriminate between the Terminals to distinguish which one will be the last to send data and therefore send the End of Transmission (EOT) signal. To accomplish this, the Multiplexer uses the cancel line which normally originates at a modem. The cancel line serves the purpose of enabling or disabling the EOT character and is also used to eliminate multiple transmission if necessary. When a terminal raises a request-to-send, if a cancel is received before a clear-to-send, the decoding is interrupted which results in the Terminal dropping the RTS signal. However, if the clear-to-send is received first, followed by a cancel, that Terminal is selected to produce the EOT.

6.5.5 Synchronous Operation in BOOT Mode

The Synchronous Controller can be used in conjunction with a remote station for the purpose of "Bootstrap" loading new programs into the TPU. Upon being presented with a command to enter BOOT, the Synchronous Controller will transfer to the Boot Controller all character information received after sync is found. When in the Boot mode, all TPU commands are processed by the Boot Controller. The Synchronous Controller provides eight data lines (B00 through B07) and a word enable signal. The NO SYNC signal indicates the Read mode has been entered but word sync has not been established. The Synchronous Controller also provides the Boot Controller with the data carrier which the Boot Controller monitors and should the carrier be lost for any reason, the error can be signaled and re-boot initiated.

6.5.6 Basic Operation

During the following discussion, schematic 001-08-01, Synchronous Modem Controller, will be referenced (sheet 1 is a cover sheet and therefore is not referenced). Sheet 2 presents both the symbolic and schematic notation for the standard line receivers and drivers. Practical limitations of the line drivers and receivers are 50 feet and conform to the RS 232 specification requiring Zin (input impedance) be maintained between 3 and 7K ohms. The NEW SYNC (if optioned) is produced when a no transmit condition exists. When the carrier drops, Q7 detects the drop and a differentiation resulting in a one millisecond pulse is generated through the driver. The result is that another receive condition is established. Since the Request-to-send is not necessary if New Sync is used, STB 52 is optioned to inhibit the RTS signal. The output of M36 stays low, inhibiting and gate M35.

Sheet 3 contains the control circuitry for the synchronous operation. Program command decoding is performed at the gates and inverters in the upper left portion of the schematic. Typical decodes are T I/O at M19, R I/O at M20, C I/O at M13 and W I/O for acknowledge (ACK) at M26. Through the middle of the schematic the circuits which remember the operation being performed and other conditions are found in the form of flip flops and latches. M59 (pins 15, 14) is the Read/Write flip flop. Flip flop M59 (pin 11) provides the mask interrupt signal. Latches M21 and M14 remember the conditions of overrun and carrier detect. The remaining logic on the right side of sheet 3 is the interrupt logic.

Sheet 4 contains the various timing elements. The counter M38 and M47 (2) is optioned at STB 15 and 16 to provide for the 6, 7 or 8 bit decode. Flip flops M38 and M29 operate as the sync code bit counter with the decode optioned at STB 23. When using an 8-bit character parity is generated for the first seven bits; the eighth bit picks up a 1 or a 0 from flip flop M29 (option block 22, pins 9 or 10). If not transmitting parity, the option is grounded. Serial data is outputted from M48.

Sheet 5 schematically illustrates the flow of data from the TPU output bus OTB 00-07 into the data buffer. The data buffer can also contain received data which has been converted from serial to parallel at registers M17 and M24. The input buffer is enabled to the parallel storage register, M12 and

M5, which outputs parallel data to either the TPU input bus, Boot Controller or Parallel/Serial Register (M17, M24).

Since the Modem operates asynchronously with respect to the TPU, the synchronous controller makes the required time translation. On sheet 3 flip flop M58 is set, through M35 and M54, by the Q side of the Read/Write flip flop (M59 pin 15) which is conditioned when a receive character is present or available. This condition is in modem time. M58 can only be clocked by the INT SEL IN signal which is when the time translation takes place. The first select in sets M58 but also conditions M54 and passes the select out. The next select that comes in will not pass because M54 is now disabled and the signal enabled is the INT SEL OUT.

6.6 SPLIT SCREEN CONTROLLER

The Split Screen Controller, unlike previously described controllers, does not require I/O and function commands from the processor. The Split Screen Controller (see Figure 6-8) is used in a configuration where an auxiliary display capability is desired. The main function, then, is to provide the video and synchronizing signals necessary for operation of the Auxiliary Display on a time-sharing basis with the Master Display. The time-sharing results in a reduced number of lines per display. Under normal or single display conditions, there are 31 displayable lines on the T. V. screen. When a Split Screen Controller is installed (normally in Slot 7), there are 15 lines available at each T. V. screen, which allows a single space in the time frame for switching. Under certain circumstances, it may be desired to disable the Auxiliary and display all lines on the Master T. V., in which case the split screen controller is removed and replaced by a jumper board.

The full dual configuration consists of a Master Terminal with keyboard and an Auxiliary Terminal with keyboard. The Keyboard Controller for the Auxiliary Display is located in the Master, usually at Location 3. The reason that the Split Screen Controller does not require the extensive I/O and function control from the TPU is that the controller does not have to operate on data. The two keyboard controllers are assigned a different priority interrupt by the program, therefore the program knows which keyboard has presented data and all the Split Screen Controller has to do is provide the timing to display the data on either screen.

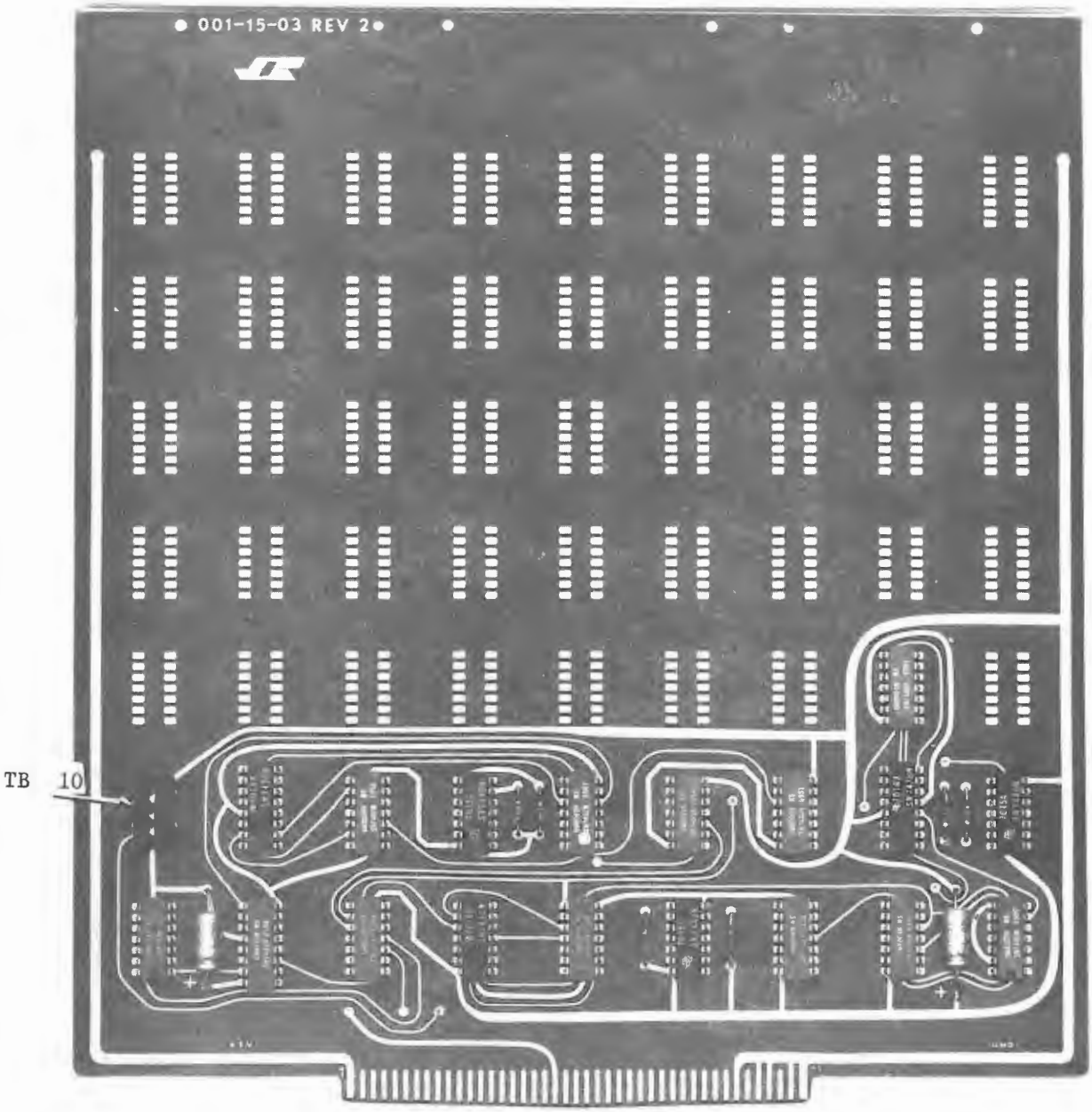


Figure 6-8. Split Screen Controller

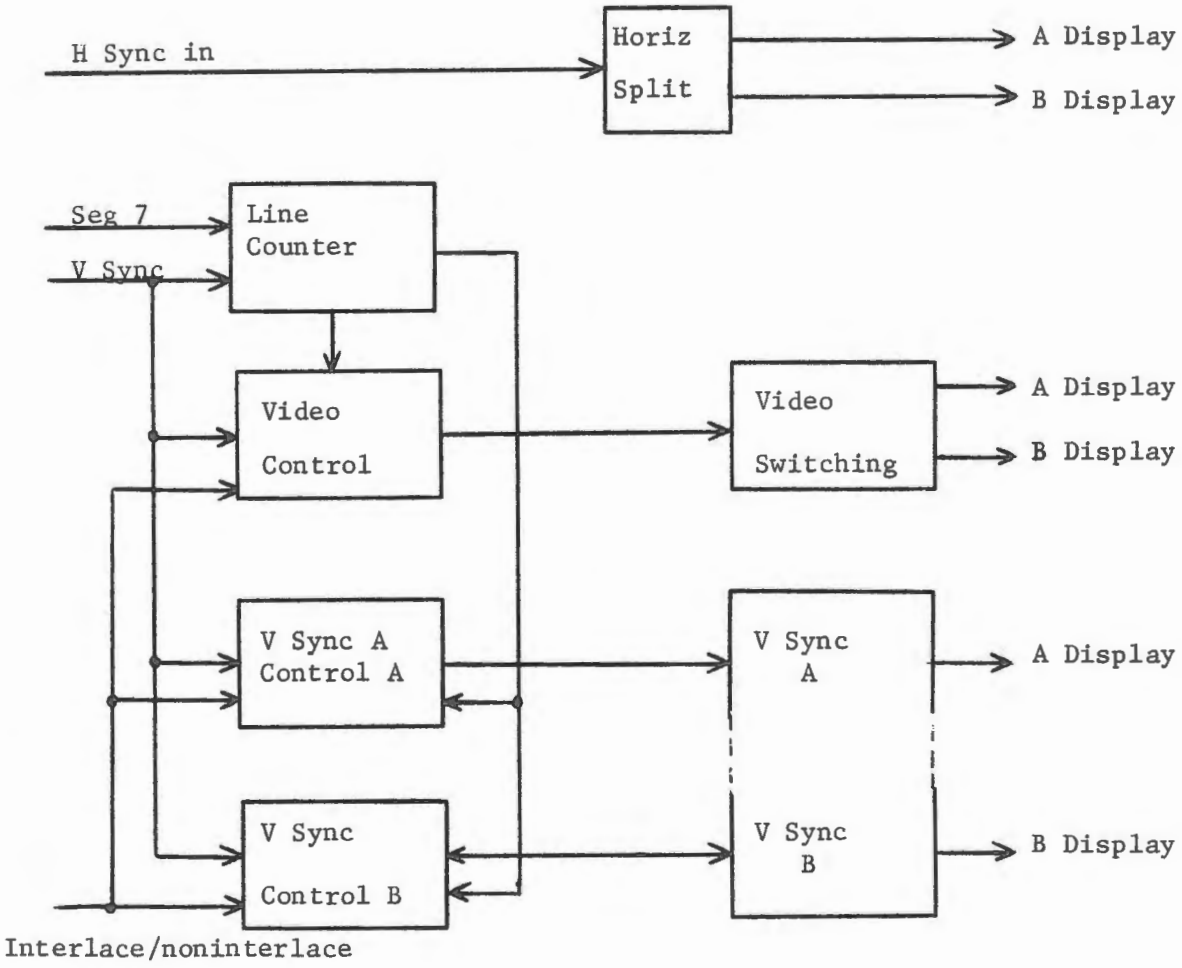


Figure 6-9. Simplified Block Diagram
Split Screen Controller

Figure 6-9 is a simplified diagram of the Split Screen electronics. Overall requirements for operation are that the line counter produces specific counts initializing at V sync time. Figure 6-10 provides a graphic representation of the split screen sync timing. The normal mode of operation provides V sync pulses every 31 lines, such that when the odd field has been displayed, a V sync resets the scan to the top of the screen and the even field is scanned. A complete display is produced after both the odd and even field data has been produced on the display.

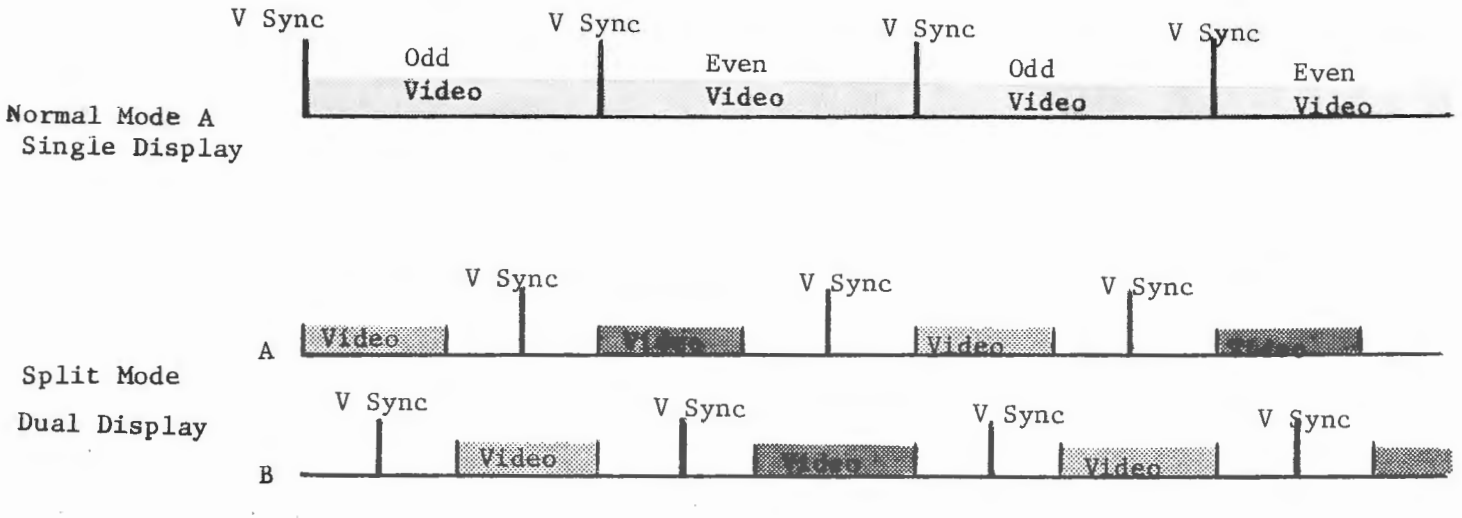


Figure 6-10. Split Screen Timing

In the split mode, the normal V sync is shifted by eight lines and precedes the video by eight lines. The video envelope is 15 lines. Note that in the normal time frame there are now two sync pulses and video to two displays.

Stated simply, the operation begins the first time the normal V sync arrives at which time the counter is set to 0 and A video is enabled. Looking at the timing diagram, when the counter reaches 8 V, Sync B is enabled after which eight more counts enable the B Display video. Notice that after the original count of eight and first shifted V sync, each successive count of 16 enables a V sync pulse which is toggled from A to B, and results in either the A or B receiving V sync at the original rate.

6.6.1 Operation

The following discussion references schematic 001-15-01. The input signal HSYNC (Horizontal Sync) is inverted at M7 and applied to gates M6 (HSYNA) and M6 (HSYNB) which, for all practical purposes, only splits the signal and feeds it back out to both displays. The video input is applied equally to 1/2 of AND gates M12 with the other half being the enable A or enable B from flip flop M11. The negative going outputs are inverted at Gate M13, from which they are provided to either display. The interlace/non-interlace signal is hard wire selectable and normal split screen operation is interlaced. However, gating is provided for non-interlaced operation. Assuming non-interlaced conditions, the gates provided would change the timing because the number of lines available would be halved. Gate M12, M14, M4 and M9 are used in non-interlaced. The remainder of the input signals are timing signals from the RMTU.

The V sync at M5 is the normal system signal which provides a pulse every 31 line counts in the RMTU. The signal output of M5 when true (low) resets the counter SURL0 through SURL4, produces the A video enable at pin 14 of M11, and sets the A and B sync flip flops through latches M19. When the counter counts up to eight (decode of seven at M2) the odd time is ANDed with the eight count at M15, which enables M16 pin 8 and produces a B sync pulse. When the counter reaches 16, Gate M4 is enabled by a 16 count on pin 1, count of 1 on pin 10, and the interlace enable on pin 9. The results are that the A/B video flop toggles and B display video is enabled. The counter continues to count up and a count of 16 and eight is ANDed at M14 and the V sync A is enabled through M9 (pins 4, 5 and 6) and M15.

The next normal V sync that comes in will toggle M11 again, turning the V video off and the A on, resetting the clock and the sequence is started over again, this time for the even field. Frame switching is performed by ANDing TURC4I with the odd field at M14, pins 2 and 3. The reasoning is that since there are two 31 line fields, the odd A video for the next frame will occur at a count of 62(2 x 31). Resetting of flip flops M17 A and B and toggle flops A and B is performed by segment decodes I2 and 3A, which are controlled by the RMTU.

6.7 BOOT CONTROLLER

6.7.1 Introduction

The Boot Controller operates in conjunction with the Synchronous Controller or Asynchronous Controller to monitor the communications line for a program transmittal. When a specific coded sequence is detected, the Terminal is reset and placed in a bootstrap mode called Boot. Each character of text in the message is sequentially placed in the Terminal core memory starting at address zero. In this manner, the Terminal program is remotely updated from the central site.

6.7.2 Remote Load Sequence

The general format of the remote load sequence consists of two BOOT characters, two ADDRESS characters, TEXT, and the END OF BOOT signal. The text portion is the actual message coming from the central site. The first four characters (two BOOT and two ADDRESS) provide the header sequence which places the Terminal in the BOOT mode. The END OF BOOT character releases the Terminal from the Boot mode. The coding for the BOOT and END OF BOOT characters is flexible; they can be implemented by hardware options and may not appear in normal text from the central site. The two ADDRESS characters are identified as ADDRESS1 and ADDRESS2 and their configuration controls the implementation of the Boot mode in a multi-terminal application. The remote load sequence can be addressed to a specific terminal (specific addressing), all terminals (general addressing) or only those terminals ready to receive it (error addressing). In addition to the specific codes for the ADDRESS1 and ADDRESS2 characters, another character code, GENERAL

ADDRESS, is used. It can be used in place of either or both ADDRESS1 and 2 characters to specify the addressing classes (specific, general and error) as described below.

Specific Addressing

Only the terminal whose Boot Controller satisfies address comparison of both address characters will be reset and placed in the Boot mode. The ADDRESS1 character is usually a site address and the ADDRESS2 character is a Boot Controller address.

General Addressing

If the ADDRESS1 and ADDRESS2 characters are the GENERAL ADDRESS characters, all terminals on the Line are reset and placed in the Boot mode. If the ADDRESS2 character is the GENERAL ADDRESS character, but the ADDRESS1 character is not, only those terminals whose address comparison is satisfied by the ADDRESS1 character respond to the remote load sequence (all terminals on a Multiplexer).

Error Addressing

Only those terminals respond that have been previously placed in the Boot mode, but have not yet received a remote load message. The ADDRESS1 character is the GENERAL ADDRESS character. The ADDRESS2 character specifies that this is the error remote load sequence. All terminals on the line that are in Boot mode load the new program.

6.7.3 Boot Controller Circuitry

The circuitry for the Boot Controller is contained on one printed circuit board. A simplified block diagram of the controller is shown in Figure 6-11. The logic for the Boot Controller is shown on drawing 001-09-01, sheets 2 and 3.

The Boot data input signals are shown on the left side of sheet 2. They are identified as B00 through B07. These 8-bits are inverted by gates M30, M39 and M48 and immediately sent to option blocks STB 31, 49, 29, 47, 28, 46, 27, 45, 22 and 19. (Refer to Appendix B for option block descriptions.) The ADDRESS, BOOT and END OF BOOT character codes are flexible and they can be specified by the wiring of the option blocks. These characters, represented by B00 through B07, are decoded by the gates and flip flops shown at the top center section of sheet 2 (M9, M18, M8, M16, etc.). This logic network generates the signal (CONT BOOT) that is sent to the TPU and puts it in the Boot mode. A valid remote load sequence is detected in the following way to generate a CONT BOOT signal.

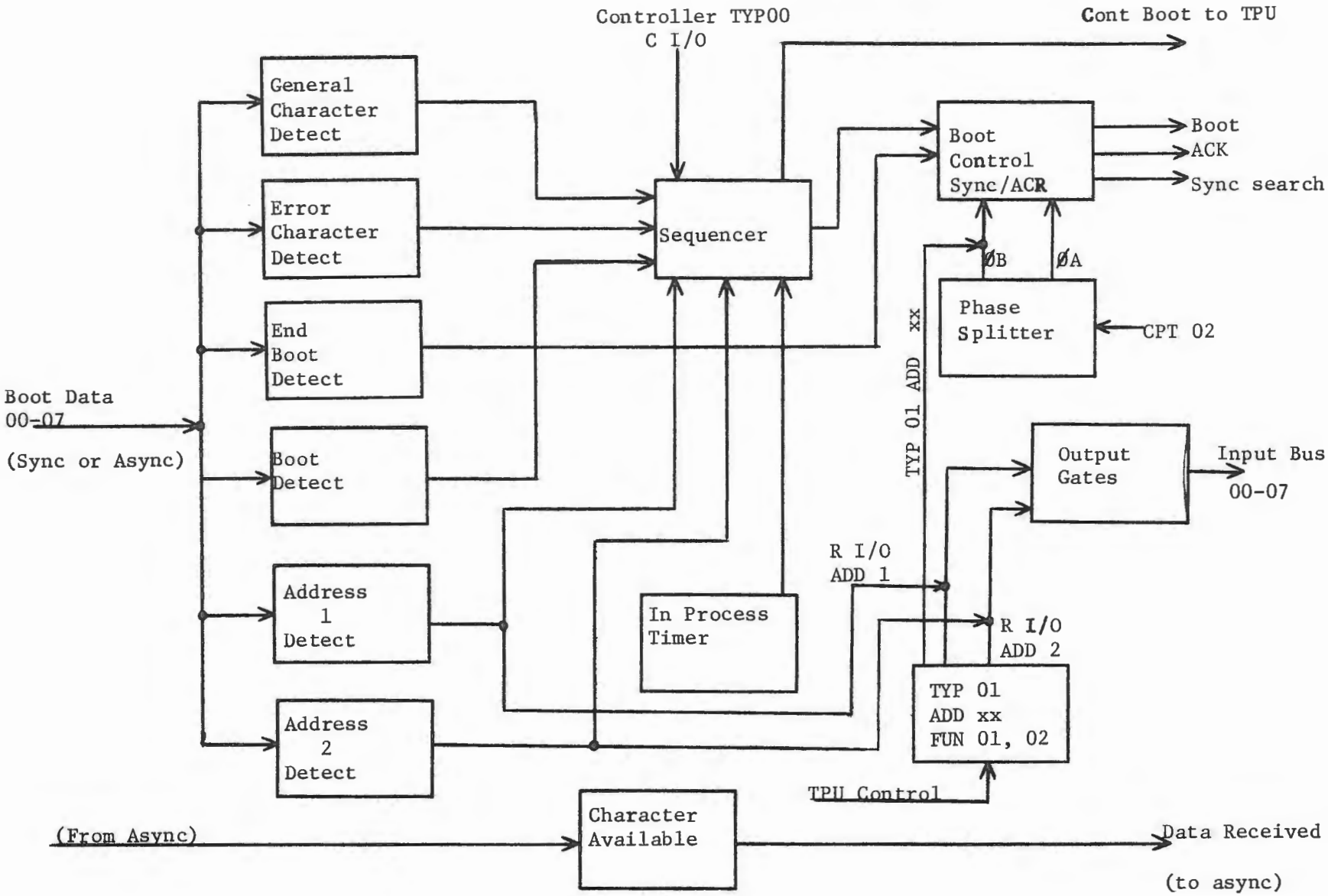


Figure 6-11. Simplified Diagram Boot Controller

a. 1st character, BOOT, sets flip flop M9 (BOOT 1)

b. 2nd character, BOOT, sets flip flop M9 (BOOT 2)

c. 3rd character, ADDRESS1 or GENERAL ADDRESS, sets flip flop M18 (ADD1/GEN)

d. 4th character, ADDRESS2, GENERAL ADDRESS or ERROR ADDRESS, sets flip flop M18 (BOOT A).

Gate M40 (BODETG) detects a valid BOOT character. Its inputs are B00 through B07 from option blocks STB31 and STB49. This gate is enabled (low) when all inputs are high. A low output at M8 (BOGCA) indicates that a character is available. Its inputs are signal CAIPHA from the Character Available logic and BOOT 2* from flip flop M9 (BOOT 2). The low outputs of M40 (BODETG) and M8 (BOGCA) are anded at M17 (BODECL) which is the clock input to J-K flip flop M9 (BOOT 1). The inputs to this flip flop are constant, J = 1 and K = 0, so that enabling the clock signal from M17 (BODECL) sets it to the one state (Q = 1). Once it is set, additional clock pulses have no effect: it can only be reset to the zero state (Q = 0) by a low signal at the Clear input (pin 3). If the next character detected is also a valid BOOT character, M17 (BODECL) is high and it sets flip flop M9 (BOOT 2) because its inputs have been conditioned (J = 1 and K = 0) by the outputs of M9 (BOOT 1). If the second character is not a valid BOOT character, the output of M40 (BODETG) is high which disables the clock gate M17 (BODECL). The high output of M40 is sent to M8 (BOOTRES) where it is anded with another high signal BOIRES via M8 (BOGCA) and M7 (BOIRES). The low output of M8 (BOOTRES) is sent to M34 (DETRES). This gate is enabled and its high output is inverted by M25 (DEIRES) and sent to the Clear input (pin 3) of M9 (BOOT 1) which resets it to the zero state (Q = 0). The detection flip flops are reset for another attempt to decode the remote load sequence.

Assume that two successive BOOT characters have been detected and flip flops M9 (BOOT 1) and M9 (BOOT 2) have been set. The next flip flop, M18 (ADD1/GEN), is set when a valid ADDRESS1 or GENERAL ADDRESS signal is detected. If this step fails, all flip flops will be reset and another attempt will be made. The inputs to M18 (ADD1/GEN) are permanently preconditioned (J = 1 and K = 0) so that a clock pulse will set it. The clock gate is M17 (ADD1/GEN) and it is enabled (high) when both its inputs are low. One

input (pin 6) is signal ADD1/GEN from the Address Decoding logic shown on sheet 3. This signal is enabled (low) if the proper code for either an ADDRESS1 or a GENERAL ADDRESS character is detected. The ADDRESS1 character is detected via option blocks STB 29 and 47 and gate M38 (AD1DETG) as shown on the lower left section of sheet 2. The GENERAL ADDRESS character is detected via option blocks STB 22 and 19 and gate M21 (GENERR) as shown on the upper left section of sheet 3. The other input (pin 5) to M17 is sent from gate M16 (BOADCA) which is enabled when its three inputs are high. The inputs are: BOOT 2 which is high when M9 (BOOT 2) is set; CAIPHA which is high when a character is available; and ADD1/GEN* which is high when M18 (ADD1/GEN) is not set. With all these conditions satisfied, M17 (ADD1/GENCL) clocks M18 (ADD1/GEN) and it is set. If the proper address code is not detected, signal ADD1/GEN is high and it is anded with the high output of M7 (BOIAD) at gate M16 (ADD1/GENRE). The output of M16 resets all flip flops via M34 (DETRES).

Assume that flip flops M9 (BOOT 1), M9 (BOOT 2) and M18 (ADD1/GEN) have been set. It now remains only to set flip flop M18 (BOOTA) to complete the validation of the remote load sequence and generate the CONT BOOT signal. Flip flop M18 (BOOTA) is set when a valid ADDRESS2, GENERAL ADDRESS, or ERROR ADDRESS signal is detected. Also, if this step fails, all flip flops will be reset and another attempt will be made. The inputs to M18 (BOOTA) are permanently pre-conditioned (J = 1 and K = 0) so that a clock pulse will set it. The clock gate is M17 (BOOTACL) and it is enabled (high) when both its inputs are low. One input (pin 9) is signal ENTBOOI from the Address Decoding logic on sheet 3. This signal is enabled (low) if the proper code for an ADDRESS2, GENERAL ADDRESS or ERROR ADDRESS character is detected. The ADDRESS2 character is detected via option blocks STB 28 and 46 and gate M37 (AD2DETG) on sheet 2. The ERROR ADDRESS character is detected at the same place that the GENERAL ADDRESS character is detected; that is, option blocks STB 22 and 19 and gate M21 (GENERR) on sheet 3. The other input (pin 8) to M17 (BOOTACL) is sent from gate M16 (BOBAG). The enabling conditions for M16 are: flip flop M18 (ADD1/GEN) set; a character is available; and flip flop M18 (BOOTA) is not set. Under these conditions, M17 (BOOTACL) clocks M18 (BOOTA) and it is set. If the proper address code is not detected, signal ENTBOOI is high and it is anded with the high

output of M25 (BOIBA) at gate M33 (BOOTARES). The output of M16 resets all flip flops via M34 (DETRES). When M18 (BOOTA) is set, the remote load sequence code has been validated and the CONT BOOT signal is enabled (low). This signal places the TPU in the Boot mode.

The logic for generating the Acknowledge signal (ACK) is shown in the right center section of sheet 2. When flip flop M18 (BOOTA) is set (indicating Boot mode), the J-input of flip flop M26 (DAFF) is high. Its K-input is always low, so the next clock signal sets the flip flop. The clock signal is CAIPHA which is the output of the Character Available logic. The high output (pin 15) of M26 is sent to pin 4 of gate M8 (ACGOUT) which generates the Acknowledge signal ACK. The low output (pin 14) of M26 is sent to pin 3 of gate M20 (ENACK) on sheet 3. The other input (pin 4) of this gate is low when the controller address signal ADDXX is low and the Type Bit 01 (TYP01) is low. With both inputs low, M20 (ENACK) is enabled (high) to pin 5 of M8 (ACGOUT) which generates the Acknowledge signal (ACK low) to the TPU. This acknowledges data to the TPU which is the text portion of the remote load sequence.

The END OF BOOT character is detected via option blocks STB 27 and 45 and gate M36 (EBDETG) on sheet 2. If the proper code for the END OF BOOT character is detected, M36 is enabled (low) to M25 (EBIDET) which inverts the signal and sends it to pin 10 of M33 (EBGBOA). Two other high inputs are required to enable M33. Pin 9 is high if flip flop M18 (BOOTA) is set and pin 11 is high if a character is available. Gate M33 (EBGBOA) is enabled (low) to M34 (DETRES) which resets all the flip flops and removes the TPU from the Boot mode.

Detection of certain conditions by the controller allows it to reset the TPU and place it in the Boot mode. One condition is related to the length of time that the TPU is in the transmit loop. It is considered a TPU failure if the Synchronous or Asynchronous Controller remains in the transmit mode longer than one minute. This condition is detected by a timing circuit in the Boot Controller which initiates action to place the TPU in the Boot mode again. The Boot Controller can be manually placed in the failure mode by the operator if a failure is detected or suspected. The manual operation consists of depressing the concealed boot switch and keying-in five characters from the keyboard.

Two other conditions, termed error recovery situations, allow the Boot Controller to put the TPU back in the Boot mode. One is detection of the loss of the carrier signal from the data modem. The other is receiving a remote load sequence prior to receiving an END OF BOOT character from the current remote load sequence.

As previously stated, if the Synchronous or Asynchronous Controller remains in the transmit mode longer than one minute, it is considered a TPU failure. Normally, a TPU is capable of handling all messages to the central site in less than one minute. Measuring of the transmit time is accomplished by the timing logic shown in the lower right section of sheet 2. The allowable time is predetermined by option block STB 23 (maximum is one minute). The output of a free-running oscillator (Q1 and Q2) is counted down by M32 and M15 to produce an output at pin 14 of M32 (TIME) that pulses once per minute. Detection of the transmit mode is accomplished by input signal XMIT MODE via gates M48 (TRANS I) and M42 (TORG). Without tracing the signals through every gate, the sequence is as follows: If the transmit time is exceeded, M32 (TIME) is set and its output (pin 10) sets flip flop M43 (BODRF) via gate M14 (DBCG). The $\overline{Q}$ output (pin 10) of M43 resets all the Boot flip flops via gate M34 (DETRES) which takes the TPU out of the Boot mode. This same output of M43 sets the RS latch composed of M24 (BOL 00) and M33 (BOL 01). The output of M24 is sent to the decoding logic on sheet 3 which allows an ERROR ADDRESS to be decoded. This output of M24 is also the BOOT signal but it cannot be passed through gate M8 (BOGOUT) because this gate is disabled by the low output (pin 10) of M43 (BODRF). However, after two TPU cycles, M43 (BODRF) is reset and the BOOT signal is enabled via gate M8 (BOGOUT). As far as the TPU is concerned, Boot has been entered. However, there is no Acknowledge signal generated until the correct remote load sequence is received which includes an ERROR ADDRESS to set flip flop M18 (BOOTA).

The Boot mode can be re-entered in a similar manner by receipt of a Command I/O from the TPU. It is decoded by the logic shown at the top right section of sheet 3. The enabled (low) output of M13 (ENTBOOT) sets the RS latch (M24/M33) which generates the BOOT signal.

One error recovery condition concerns the detection of the loss of carrier signal during Boot operation. The loss of carrier signal is detected at pin 69 which is the input to gate M17 (CDIBC). When this input is low, there

is no carrier signal and flip flop M43 (BODRF) is set via gate M14 (DBCG). The sequence of action from this point on is the same as that described in the excessive transmit time condition.

Another error recovery condition concerns the receipt of another BOOT character prior to the processing of the BOOT characters in the current remote load sequence. If this situation occurs, the Boot flip flops are reset for another attempt.

Synchronizing takes place concurrently with the Character Available line (input pin 59) which is a pulse from the Synchronous or Asynchronous Controller that identifies the presence of a character. The two controllers behave a little differently in that the pulse count timing is slightly different. The synchronizing logic provides the correct pulse time to use with the Boot Controller. The Asynchronous Controller has a further requirement that the Synchronous Controller does not have. When the character is available, the Asynchronous Controller requires a response pulse that indicates the Boot Controller has accepted the character. Due to the way the asynchronous logic is arranged, a flip flop which is set must be cleared out. In the Boot mode, there is no way of getting it cleared out so essentially the Boot Controller feeds back the same character that is used to clear out the flip flop. There is one signal that is peculiar only to the Synchronous Controller and that is the FIND SYNC signal (connector pin 57). If the Boot Controller puts the TPU into the Boot mode, the Synchronous Controller must be signalled to do a sync search. On sheet 3, STB 10 (ADD2TB) and 11 (ADD1TB) are connected into the input bus of the TPU. After leaving the Boot mode, the TPU issues a Read I/O to the Boot Controller and the output gates provide the ADDRESS1 and the ADDRESS2 signals in accordance with the wiring of the option blocks. Option blocks AAD1TB and ADD2TB must be wired to the same address as the option blocks for ADDRESS1 (STB 29 and STB 47) and ADDRESS2 (STB 28 and STB 46) shown on sheet 2.

CHAPTER VII

MAINTENANCE AND REPAIR

7.1 GENERAL

The maintenance and repair philosophy for the SPD 10/20 Terminal provides for several functional considerations. An on-line terminal can be repaired by the substitution method in the shortest possible time; therefore, the substitution method is recommended. The Field Engineer carries to a site a known good complement of TPU circuit boards. Such items as cables and I/O circuit boards are generally at the customer site in the form of a spare unit. With the exception of power supply voltages, test point monitoring within the TPU is not practical at this time. If the substitution of boards is successful, the defective circuit board is returned to a depot for repair at which time test points are utilized.

7.2 FIELD SUBSTITUTION

The SPD 10/20 Terminal provides many visible indications pertinent to operating problems. The CRT can be used as an indicator and observing Program Loader operation, along with expected results, can also provide indication of a problem area. Table 7-1 lists some possible problems along with a probable cause analysis.

Power Supply voltage checks are taken without removing the supply from the terminal chassis. Figure 7-1 illustrates the terminal face down which exposes the power supply for voltage checks as follows:

Table 7-1. Field Problem Identification

Problem	Probable Cause
Will not load past last boot character	Defective DATA CONTROL board, or KYBD Control Board. Defective MEM. ELEC., MEM. STACK, or Data Flow. P/C board misalignment (incl. controllers). Program might have to be reloaded a second time in the event of a blown program. Broken wire to Interrupt Select Signal. Missing Controller Board.
Program loads past end of tape.	Defective DATA CONTROL, RMTU, MEM. ELEC., MEM. STACK, DATA FLOW, or Paper Tape Reader.
Cannot load program tape.	+14V lower than +13.5V (check thermister on stack). Missing DC voltage/defective P.S. board. Defective MEM. STACK or DATA FLOW board. Defective P.T. (blown output transistor in P.T. reader) reader or cable. P/C board not completely seated. Defective DATA CONTROL, MEL., or RMTU board.
Displaying incomplete characters, numerous random characters or screen full of same character.	Defective RMTU.
Horizontal positioning too far to the left.	Adjust trim pot at base of monitor. (See Monitor adjustment procedure.)
Terminal not being polled from central site.	Defective I/O controller. Defective MODEM or incorrect type. Check MUX if one is used. Check I/O cable. Incorrect option blocks.
Program hang-up—cannot XMIT, cannot enter or clear data.	Turn power OFF and back ON. If it persists, check TPU electronics or I/O Controller (Data Flow/Control).
Program consistently being destroyed.	Defective CPU Control Board (Check C5). Defective MEM. ELEC. Defective power supply ("B" brd). Defective RMTU (will not go into Clk stop).

Table 7-1. Field Problem Identification (Cont.)

Problem	Probable Cause
No power save. (Load program, push red Boot button on SPD 10/20, type in "kool 7." Cursor should reappear, if it does, problem is isolated to #4, 7.)	Broken wire to P.S. Defective capacitor (C5) on Data Control Bd. Defective Data Control Board. 4) Defective MEL Noisy or defective power supply boards. Defective RMTU 7) Defective "B" board in P.S. PWR-UP line not properly connected from P.S. to A14 Pin 69.
Raster wavers.	Adjust vert. sync on monitor. No +5V (Bad P.S.) Sync problem in RMTU. Bad split screen board. Defective monitor. Defective line lock circuit.
Not displaying character depressed on keyboard, but other characters work.	Defective RMTU KYBD. cable partly disconnected or defective Stuck key on KYBD. Defective KYBD. controller. Defective switch on keyboard. Defective I/C in KYBD. electronics. Broken or intermittent connection.
No Characters.	Defective KYBD. (no strobe)
Previous characters on display change as new ones are typed in.	Defective RMTU.
Multiple cursors displayed on CRT.	Defective RMTU or DATA CONTROL. Defective DATA FLOW or I/O Controller, or wrong program/controller set-up.
Double or no cursor.	RMTU
No video.	Loss of -14V or +25V to ROM. (2N5188 on RMTU Bad, caused by shorting to back of CPU Control board.) Bad Split screen board. Loss of +14V to MEL address (no drive current to monitor).
No Blinking cursor (hardware function).	Broken jumper wire on RMTU board (M104-10 to M94-11).
Program not functioning properly on line.	Defective I/O Controller.

Table 7-1. Field Problem Identification (Cont.)

Problem	Probable Cause
Constantly blowing output transistor in program loader.	Missing voltage to program loader. Defective RMTU (never plug in Loader without RMTU Sync.) Check option block on RMTU. TURT4 signal missing. (RMTU)
Program loader solenoid operating at irregular speed or not advancing tape.	Loading of +14V to P.S. (J9 Pin 38). Interrupt select floating. (Any Controller)
Displaying double characters.	Defective RMTU board.
Programs blowing frequently.	Static electricity present in room, possibly from nylon carpeting. (Reload Program) Noisy P.S. boards.
No. D.C. voltages.	AC fuse blown. Interlock switch not fully engaged. AC wiring to MOLEX connector has bad connection or pin vibrated loose. Power supply boards not firmly seated. Defective P.S. boards or P.S. chassis.
Missing D.C. voltage.	Blown fuse. Intermittent connection to P.S. Defective P.S. boards or P.S. chassis.
P.S. 25V at 35V.	Defective thermister on MEM. STACK. No regulation from P.S. "B" board.
Oversized raster, terminal out of sync, and high frequency pitch from terminal.	Option block on RMTU board. Defective RMTU.
Solid line appears on CRT.	Defective power transistor (MP 3730) in monitor. (Deflection Amplifier)
Cursor moves randomly across screen.	Defective RMTU.
Half raster displayed on screen.	Defective RMTU. Defective split screen board.

Table 7-1. Field Problem Identification (Cont.)

Problem	Probable Cause
Sonalert doesn't work.	Defective KYBD Controller. Defective DATA CONTROL BOARD. Defective SONALERT. Broken wire. Blown program.
Raster looses sync when loading program.	Heavy current drawn from +14V. (Defective supply)
No brightness on Monitor.	No 117 VAC - check MOLEX conn. on P.S. Circuit breaker open (interlock switch). Defective high voltage rectifier in P.S. Check connection on back of CRT. (socket).
Program loader solenoid is activated when unit is turned on.	Defective "B" board in Program loader. Bad CPU Control Board.

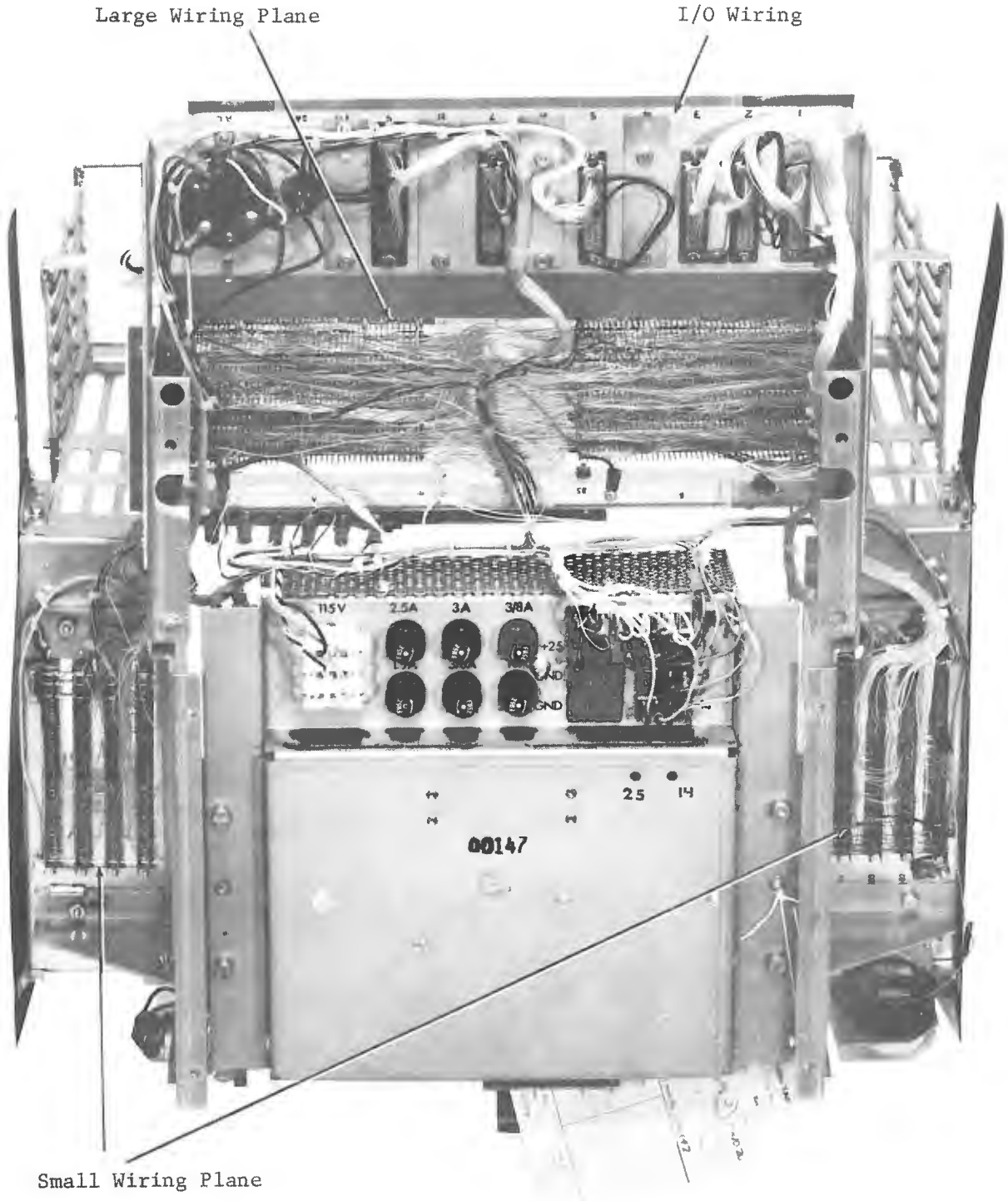


Figure 7-1. Bottom View of Terminal Illustrating Voltage Test Points and Adjustment Locations

Connector	Voltage
Brown	Thermistor connects across these two wires—the thermistor is located on the stack, board 11.
Yellow	+5
Red	25
White	+5 (for power up)
Blue	-14
Black	Ground
Green	- 5
Orange	+14
Clear Nylon	115 Volts ac

The +14 and +25 Volts can be adjusted by inserting a screwdriver (thin shaft) in the potentiometer holes located and identified in Figure 7-1.

The previous test points provide information relative to the power supply output.

Suspected failures external to the system such as faulty Tape Reader, Keyboard or their associated cables can be substituted with known good elements to verify whether a fault condition exists. A high percentage of keyboard faults can be traced to a defective reed switch. Isolation of the faulty switch is not difficult and replacing the switch is not time consuming. Therefore, field replacement is practical. The following procedure can be used to locate and replace a faulty reed switch: (See Figure 7-2.)

1. Dismantle the keyboard outer housing by removing the four exposed screws on the bottom of the keyboard. The bottom plate can now be removed.

2. Remove the keyboard from the retaining brackets by removing the four mounting screws. The PC assembly can now be removed from the housing.

3. Place the two leads of a voltmeter across the suspected switch points. With the voltmeter placed to the ohms scale, depression of the key top should cause meter needle deflection. If the meter does not deflect or is constantly deflected, the switch is either open or shorted.

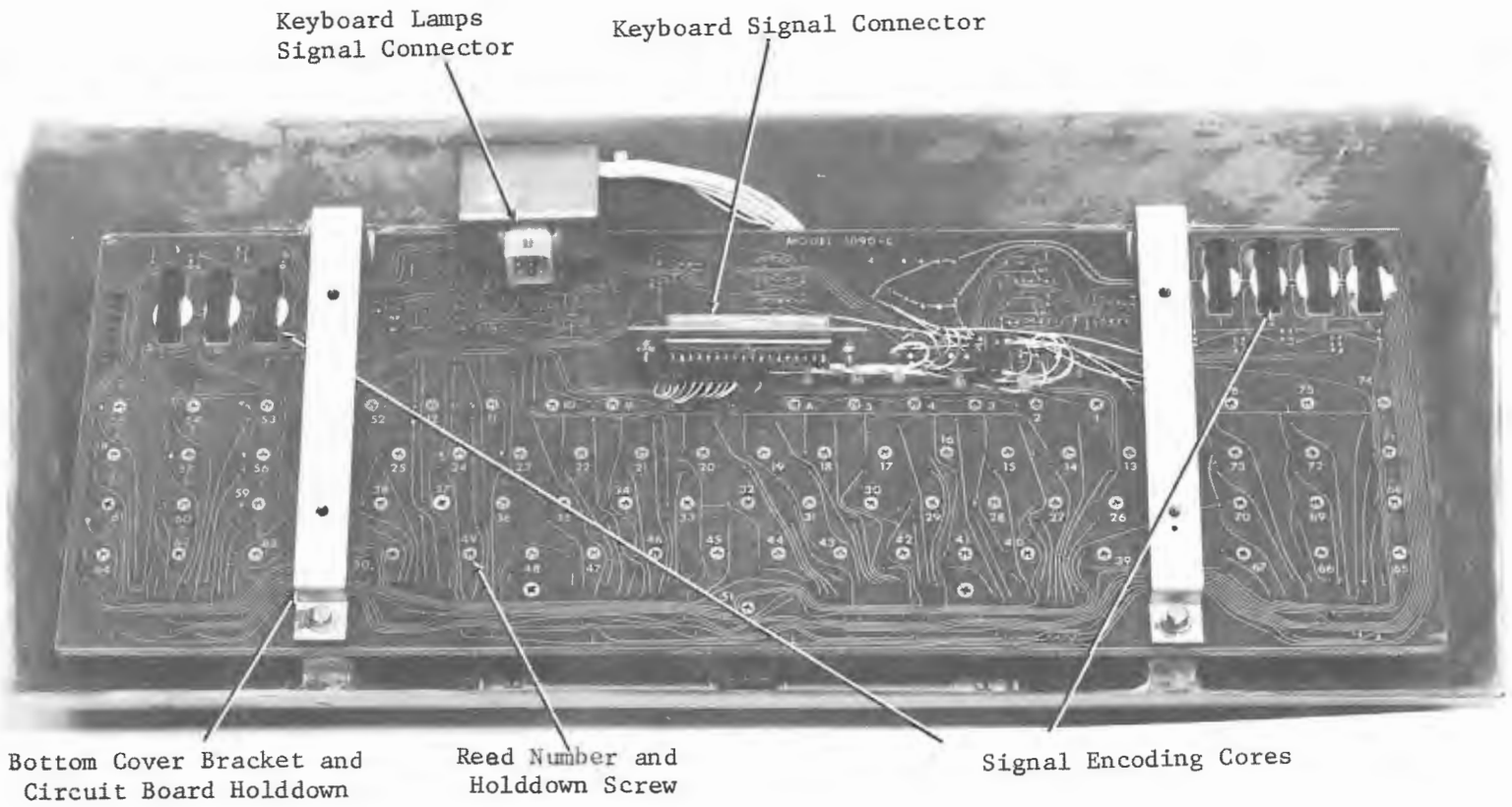


Figure 7-2. Keyboard Bottom View

4. To replace the switch, remove the phillips head screw from the switch and unsolder the two switch connections.

5. The switch can now be removed from the circuit board.

6. Replace the switch by reversing the removal procedure.

7. When replacement is complete, the key top of the removed switch can be removed from the actuating rod and placed on the new switch. (No tools are required for this step.)

Defective circuit board repair is accomplished by observing various test points within the terminal processor. For overall effectiveness and time-to-repair considerations, a test console is used to monitor and display the essential digital signals within the terminal processor. Prior to a listing of the test points, the following introduction to the operation and use of the test console for hardware problem isolation is provided.

7.3 TEST CONSOLE

The test console, as illustrated in Figure 7-3, is composed of an array of lamps and a group of toggle switches. The lamps are dual purpose in operation and are used both as a read-out device and a switch. As illustrated, the lamps correspond to previous discussions relative to the names of the different data registers and the number of bits contained. For example, the top row of lamps corresponds to the 16 bits of the Memory Data Register. A lamp, when lighted, is amber in color and represents the bit as being set (1). The switch action allows the bit position to be manually set by depressing the lamp lens inward. The white lamps are not wired to produce a lighted condition, but are used as a switch. Depressing a white lamp clears (resets to 0) the register associated with it. Except that the AAR, MAR and PCR are interrelated when performing the "clear" operation. Depressing the "clear" button for the MAR or PCR will transfer the contents of the AAR to that register. In order to clear the MAR or PCR, the AAR must first be cleared, then the MAR or PCR. The toggle switches will be explained in their respective order of use after the test point connections are discussed.

Test Points - test points are provided on the etched circuit boards in the form of 14 pin pads. The connection between the terminal and the console is via 14 conductor ribbon cable. The following test point identification is for the 005 and 006 test console.

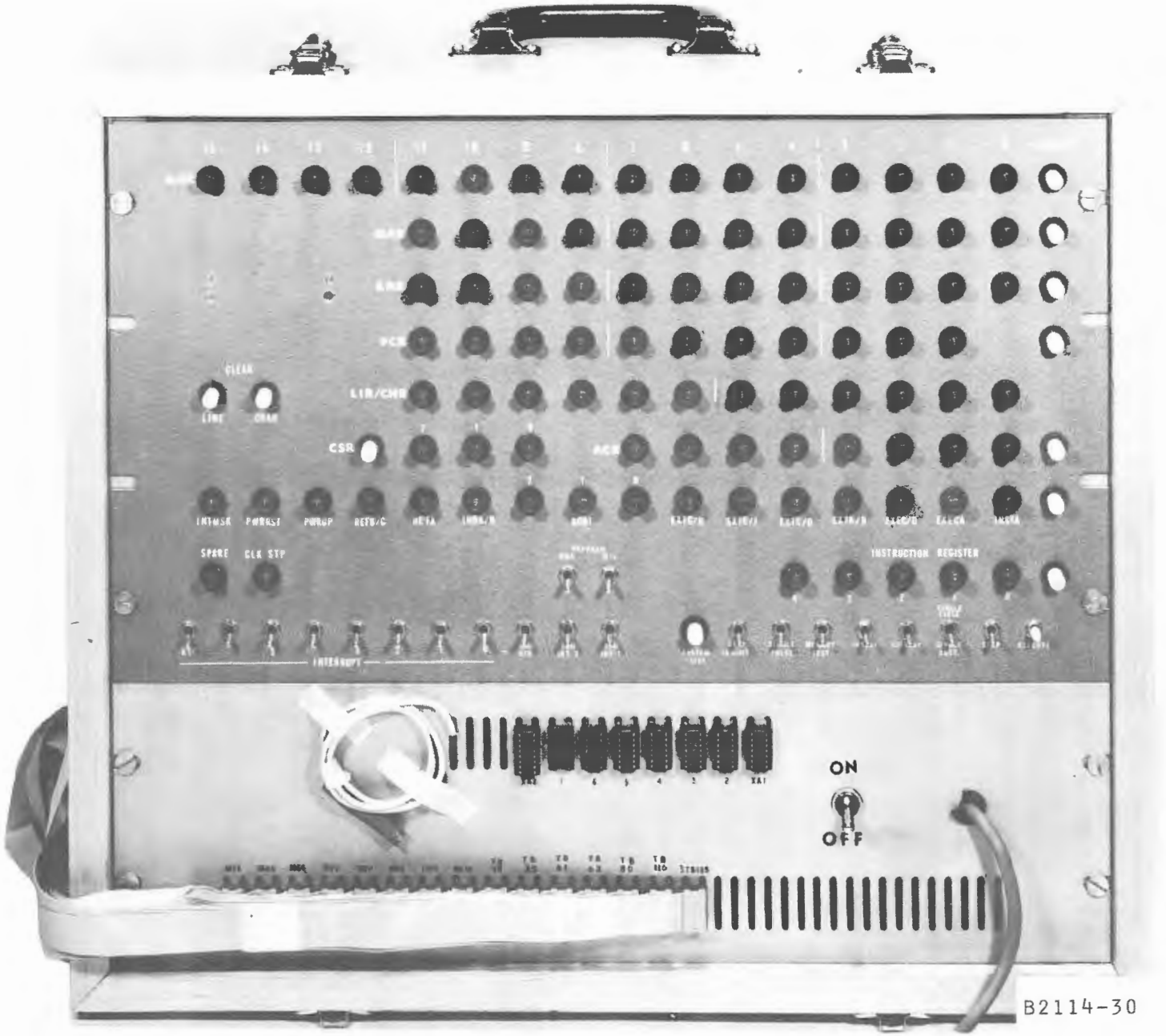


Figure 7-3. INCOTERM Test Console

RMTU, SLOT 14, 005-14-03 REV A

The RMTU has one ribbon cable run to it. Figure 5-13 illustrates the component side of the RMTU and calls out the socket for the connection STB 105. This point is brought over to the console solely for the purpose of enabling the modes of operation involving clocks such as clock stop, single pulse, single cycle enable and refresh enable/disable.

CONTROL BOARD, SLOT 13, 005-07-03 REV 1

The control board is connected to the console by six ribbon cables connected to the test blocks illustrated in Figure 5-4 which locates each test block. The test signals from the control board are applied to some of the toggle switches and all of the lamps on the bottom two rows of the console.

DATA FLOW, SLOT 12, 001-02-03 REV 1

The Data Flow Board is the board that creates the difference between the 005 and 006 series as far as console testing and board compatability are concerned. The difference is that the 006 eliminates test block 115 (see Figure 5-3), which results in essentially two different consoles, one for 005 and one for 006. The data and method of operation remain unaffected.

The signals from the Data Flow test points provide a visual indication at the six topmost rows of indicator lamps. On the 005 board there are eight test block locations and on the 006 there are seven test block locations. Table 7-2 summarizes the test point connection from the terminal to the console.

7.3.1 Wiring Procedure

The normal in use console does not require removal of any wires on the console end of the ribbon cable. The terminal end of the cable is marked with its respective TB number. At the terminal end, insertion of TB plugs into the proper socket is accomplished by removing the 3 circuit boards. After the connections are made, the boards can be returned to the proper slot. Any suspected bad circuit board can be placed on an extender for the purpose of probing with an oscilloscope probe. Figure 7-4 and 7-5 illustrate both the single and dual connector extention boards.

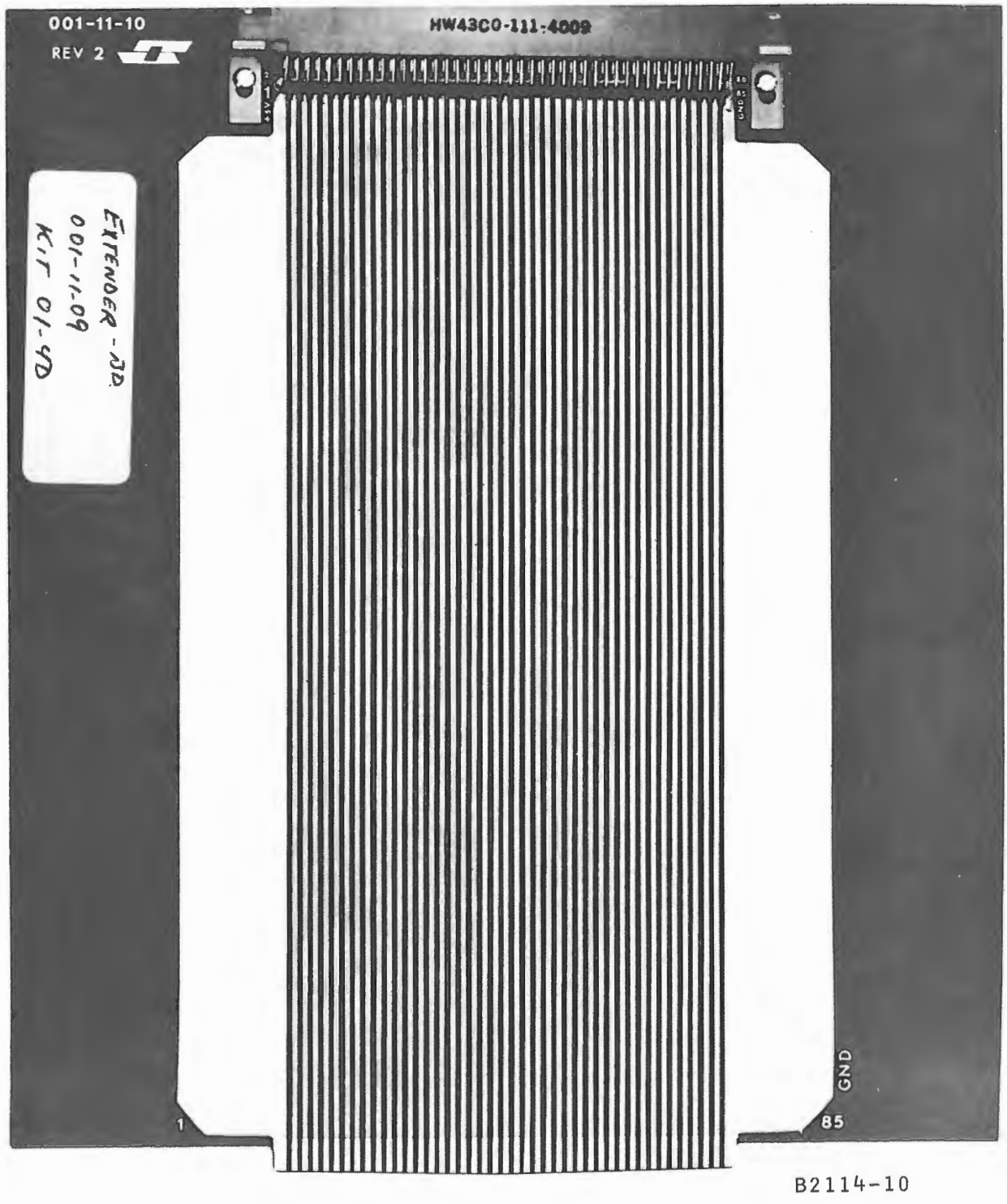


Figure 7-4. Controller Circuit Board Extender

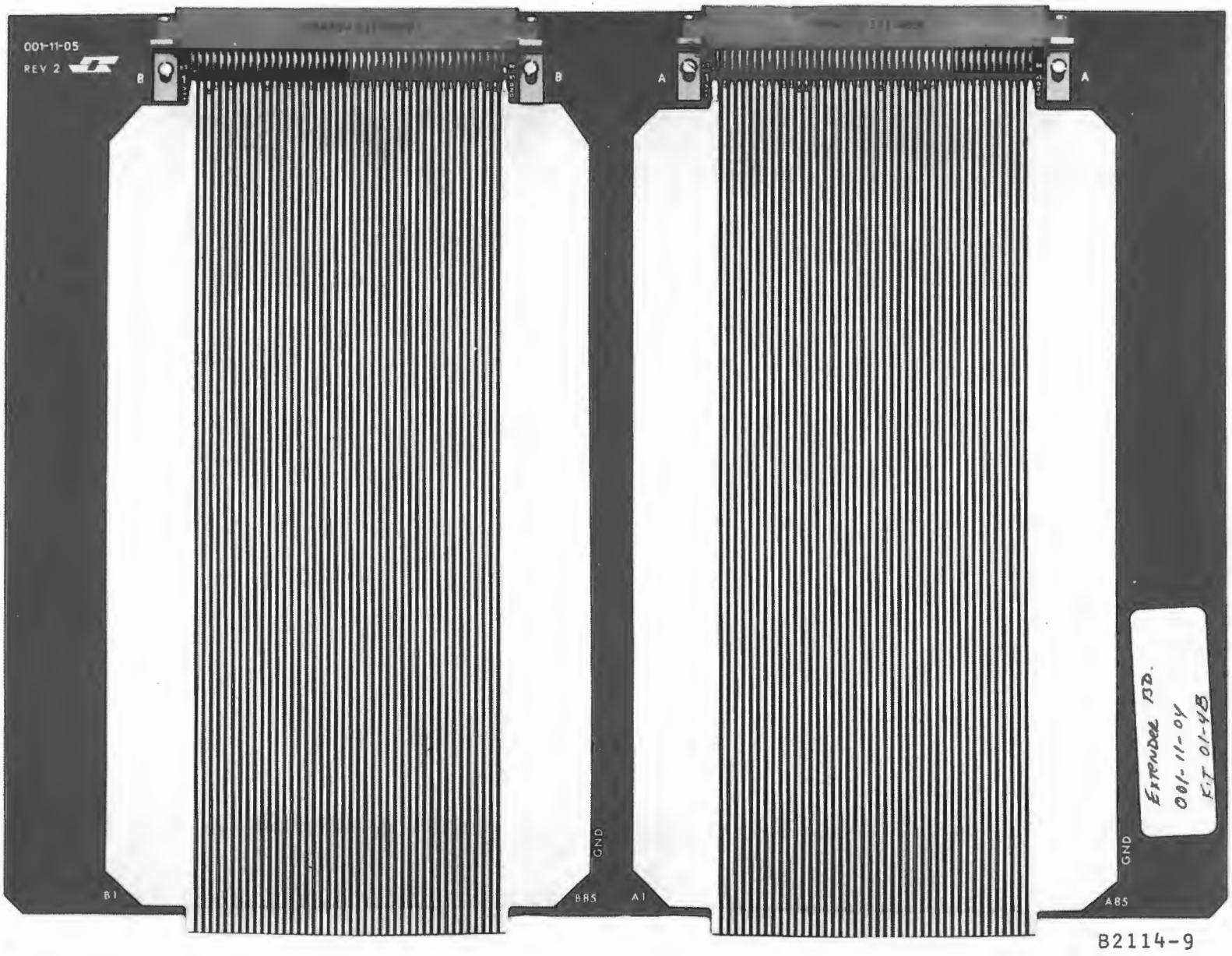


Figure 7-5. Computer Circuit Board Extender

Table 7-2. Test Point Wiring from TPU to Console

FROM		TO	
Circuit 005	Board TB 006	Console Input Position 005	006
RMTU STB 105	No Change	STB 105	No Change
Data Control	No Change		
TB 4	No Change	TB 4	No Change
TB 5	No Change	TB 5	
TB 6	No Change	TB 6	
TB 7	No Change	TB 7	
TB 8	No Change	TB 8	
TB 9	No Change	TB 9	
Data Flow			
TB 36	TB 7	TB 36	TB 7
TB 48	TB 16	TB 48	TB 16
TB 64	TB 20	TB 64	TB 20
TB 80	TB 47	TB 80	TB 47
TB 82	TB 85	TB 82	TB 85
TB 96	TB 119	TB 96	TB 119
TB 98	TB 122	TB 98	TB 122
TB 115		TB 115	

Operation - Before applying power to either the terminal or console, verify that all processor boards are in place:

Memory Electronics in	slot 10
Memory Stack (core)	slot 11
Data Flow	slot 12
Data Control	slot 13
RMTU	slot 14

There need not be any I/O controllers installed at this time.

To apply power, turn on the console FIRST, followed by the terminal power. When powering down, turn the terminal off first. After power up, the console should be placed in an initial state devoid of data. To accomplish this, proceed as follows:

1. Position the STOP and SINGLE CYCLE switches up with all others down. Note that the execute switch is a spring loaded center return switch. The center position is normal for this step.

2. Depress the SYSTEM RESET button, then all register CLEAR buttons. All lamps should be extinguished except the CLOCK STOP which is lighted. Clearing the AAR, MAR and PCR is conditional. The AAR must be the first to be cleared. The reason is that a true clear is really not done in this case. What happens is that the contents of the AAR is enabled to the PCR and MAR when their respective clear buttons are depressed. If the AAR is cleared to all 0's then the zero state is set into the MAR and PCR which results in an effective clearing of these registers.

3. The ability to enable the AAR to the PCR and MAR can be exercised to verify that data can transfer between these registers. The Reset (0) has been transferred in step 2 above, now the AAR should be set to all 1's and transferred to the PCR and MAR which will be all 1's (lighted).

4. Depress each state lamp followed by a depression of the clear lamp. This tests the operational ability of the state registers. The lamps are located in the row which starts with INT MSK on the left side.

5. Continue the register testing by depressing the INSTRUCTION REGISTER lamps. If operating properly, they will all light. Depress the clear button to clear the INST REG lamps.

6. In order that no data in the memory conflicts with further testing of the TPU, the console provides a method of clearing the memory. This also indicates the operational readiness of the memory and associated electronics. First to insert all 0's in memory set the MDR to all 0's. Then position the INSERT switch to the up position followed by positioning the STOP INHIBIT switch up. Zeros will be inserted very fast, so after a second or two the switches can be returned to the original position in the reverse order. First return the STOP INHIBIT switch to the down position followed by the INSERT to a down position.

7. The contents of memory can also be displayed on the console. This provision allows a verification that all memory positions can be set to zero (as in step 6. above) or ones if desired. To display the Memory contents position the DISPLAY switch to the up position then the STOP INHIBIT switch to the up position. If in fact all zeros had been entered the MDR will display no lighted lamps. If 1's had been inserted the MDR will display ones in all positions. To remove the console from the display mode, position the STOP INHIBIT switch to down and the DISPLAY switch down.

If all indicators have been normal up to this point, a program can be loaded into the TPU. If an indicator has not been normal such as a bit not being cleared or set, the schematic diagram for the register should be referenced and an oscilloscope can be used to probe the pertinent flip flop while depressing the set or clear button as the case may be.

If a program is to be entered into the TPU some factors which determine the success of isolating and repairing any given problem will depend upon the console operator's knowledge of how the program functions and what instructions are involved. The Programmer's Reference Manual should be referenced and a run listing of the program should be available.

To enter a program via program loader SPD-L, place the perforated tape in the operating position on the loader. Depress the red BOOT switch. Then on the console place the STOP and SINGLE CYCLE switches to the down position. Next depress the EXECUTE button or switch. The BOOT state lamps on the console will indicate a BOOT state and the tape will load data into the TPU.

Assuming the operating program is some form of diagnostic a halt instruction may be provided if an error is detected; obviously this is a programming consideration. With a fault detected the following is an example of problem isolation.

Assume the problem occurs with an instruction that provides for TPU operation in the "same sector" of memory but by observing the AAR and PCR lamps the instruction is not followed and top sector is called for.

1. First disconnect the program loader from the TPU.
2. Remove the memory electronics circuit board from slot 10.
3. Position the SINGLE CYCLE and CLOCK STOP switches to the up position.

4. Position the SINGLE PULSE and STOP INHIBIT switches to the up position. The console can now be used to step through an instruction or execute phase (20 clock pulses), one clock pulse at a time.

5. Recall there is now no Memory Electronics circuit in the TPU so the operator must simulate the data from memory by stepping past T4 (depress the execute switch five times), then manually place in the MDR the instruction that was not carried out. Now each depression of the execute switch will provide only one clock pulse and the movement of data can be readily observed at the console lamps.

6. The console operator can observe the sector Bit (9) when it drops from the AAR and also note that the bit is now missing from the PCR. From the discussion dealing with sector bits in the theory of operation it can be concluded that the PCR has in fact transferred the wrong information in Bit 9 to the AAR.

7. The hardware which enables this operation is located on the Data Flow schematic 001-02-01 sheet 31 (Program Counter). Component M1 and AND gate is labeled with the operation which it enables, that being the TOP SEC enabler. The gate then is suspect and an oscilloscope can be used to observe the output and input levels. Observe that one leg of the input is enabled through an option block and the input signal is from the bit position in question. With the scope on M1, pin 8 and an indication of a low signal, the reason the console lamp went out is verified, now the inputs to M1 are observed. The option block is located in position M14 and can be visually checked for proper wiring and insertion in the socket. The scope indication of a high on the pin 10 input to M1 and a low originating at the PCR bit register therefore indicates the option block or its connection to the circuit board is open and has caused the fault detected at the console.

This is but one example of the many possible faults, however, the signal tracing is similar for all fault isolation.

7.3.2 Detailed Explanation of Control Switches

Power-On

Power-on will apply ac power to the supplies in the console. The console must be turned ON before the TPU is turned ON and turned OFF only after the TPU is turned OFF. Up is the ON position of this switch.

Refresh Enable/Disable

Refresh Enable, when switched up, will enable refresh regardless of disable commands from the TPU.

Refresh Disable, when switched up, will disable refresh regardless of commands from the TPU.

The normal position for these two switches is down.

Interrupt

Interrupt switches RTC, 6–0 should not be used for program debug. They should always remain in the down position.

Inhibit RTC

This switch will inhibit the Real Time Clock interrupt when in the up position. Normal operation is selected by the down position.

Inhibit Interrupt 2

This switch prevents the TPU from recognizing incoming interrupts from the Controllers and the Real Time Clock.

Normal operation is the down position.

Inhibit Interrupt 1

This switch, when in the up position, will inhibit the generation of Interrupt Select signals to the Controllers and the Real Time Clock.

System Reset

When this button is pressed, it will cause an I/O reset and clear the internal states of the TPU as well as clear all registers except the ACR and MDR. For this reset to be effective, the "Execute" switch should be actuated twice since some functions AND this signal with internal timing. The TPU should be in the Single Cycle mode when this operation is performed.

Stop Inhibit

When this switch is up, the TPU will not go into clock stop regardless of the position of the Stop or Single Cycle Switch or the execution of a Halt instruction. In this mode, a Halt will be treated as a No-Op. The normal position for this switch is down.

Single Pulse

This switch must never be placed in the up position with all boards installed. It causes the clocks to advance one clock pulse at a time which could damage the unit. Always leave this switch in the down position.

Memory Test

This switch should not be used and should remain in the down position.

Insert

The purpose of this switch is to enable data to be inserted into the memory. The switch is used in the following manner:

1. Stop the TPU by placing the "Stop" and "Single Cycle" switches in the up position. Be sure the "Stop Inhibit" switch is down before attempting this operation.

2. Using the white "clear" buttons, clear the Instruction Register, Internal States, AAR, PCR and MAR in that order.

3. Put the "Insert" switch in the up position.

4. Enter the address at which the data is to be entered in the MAR.

5. Enter the data to be inserted into the MDR.

6. Actuate the "Execute" switch once. The data will be entered into memory and the address in the MAR incremented by 2 bytes (1 word).

7. If sequential addresses are to be modified, the data in the MDR only need be changed as the execute switch will increment the MAR each time data is inserted into memory.

8. To set a new address in the MAR it is necessary to put the "Insert" switch in the down position and clear the AAR and then the MAR before the new address is inserted. The proceed from Step 3.

9. To resume the program after an "Insert" operation, put the Insert switch in the "down" position, clear the AAR and insert the program starting address into the AAR. Then press the clear for the MAR and PCR to transfer this data to those registers. Then actuate the execute switch with the stop and the single cycle switches in the desired position.

Display

This switch enables the contents of the memory to be examined. The switch is used in the following manner:

1. Perform Step 1 and 2 of the Insert procedure.

2. Put the Display switch in the up position.

3. Enter the address to be displayed into the MAR.

4. Actuate the execute switch once. The contents of the memory will be transferred to the MDR and the MAR will be incremented by 2 bytes (1 word). To examine the next address, actuate the execute switch.

5. To examine a new address it is necessary to put the Display switch in the down position and clear the AAR and MAR before the new address is inserted into the MAR. Then proceed from Step 2.

6. To resume the program, place the display switch in the down position and proceed as in Step 9 of insert.

Single Cycle/Single Instruction

This switch will stop the TPU clocks in the up position if the stop inhibit switch is down. The single cycle position of this switch allows one cycle of 20 internal clocks each time the execute switch is actuated.

The single instruction position of this switch will not stop the TPU unless the stop switch is in the up position. In this mode (Single Instruction, Stop) the TPU will halt at the end of each instruction cycle. It will not halt during refresh in this mode, only at the completion of an instruction. Each actuation of the execute switch will cause the TPU to execute one instruction in this mode. To resume normal running of clocks, place the stop switch down and the single cycle/single instruction switch in the down position and actuate the execute switch once.

Execute

This switch causes a burst of 20 internal TPU clocks or the execution of one instruction each time it is actuated.

7.4 TEST POINTS NOT CONSOLE TESTED

The preceding test points provided for test console operation, include all signals necessary for maximum console performance. There are, however, additional test points located on the circuit boards to facilitate final performance testing utilizing computer aided test equipment which isolates circuit faults down to the single IC level. Table 7-3 identifies the location number, pin designation, signal and voltage level for the various TB's. Table 7-3 should eliminate any confusion relating to TB (test block) locations and STB (option block) locations.

Table 7-3. Test Points Not Console Tested

RMTU Board Slot 14

TB 19

Pin	Signal	Signal Level
1	Blink	L = Blink decode 70
2		
3	RMSCA1*	H = Code/CCR
4	RMSCA1	H = Vector/CCR
5	VGG 71	H = Char or Cur video input
6	RMSCB1	H = CCR/CDR
7		
8	CCI 13	L = Space
9	RMSCC1*	H = Character Mode
10	RMSCB1*	H = ROM/CDR
11	RMSCC1	H = Vector Mode
12	Vector	L = Vector Enable
13		
14		

TB 55

Pin	Signal	Signal Level
1	STR 01	H = Character bit 01 set
2	STR 02	H = Character bit 02 set
3	V SYNC	L = V sync
4	VSG 04	H = V sync count
5	REFREQ	H = Refresh to TPU
6	SDIG	H = Character segment data
7	VSG 03	H = V sync count
8	TURS 2	H = Time segment 2
9	TURS 0	H = Time segment 0
10	TURS 1	H = Time segment 1
11		
12	STR 03	H = Character bit 03 set
13	STR 00	H = Character bit 00 set
14	STR 04	H = Character bit 04 set

H High (+)
L Low (0 volts)

Table 7-3. Test Points Not Console Tested (Cont.)

RMTU Board Slot 14

TB 101

Pin	Signal	Signal Level
1	CUR 02	H = Cursor non display
2	TURC1	L = Char. count to AAB 02
3	CUG 00	L = Stop cursor
4	TURC2	H = Char. count to AAB 03
5	TURC4	H = Char. count to AAB 05
6	CAGR 05	L = ROM 1-0 bit A
7	CAG 00	L = Timing Reg. clock
8	CAGR 00	L = ROM 1-0 bit A
9		
10		
11	CUR 00	H = Cursor non display
12	CDR	L = Character bit 6 set
13	CDR	L = Character bit 5 set
14	CDR	L = Character bit 4 set

TB 103

Pin	Signal	Signal Level
1	CSG 33	L = Clocks sequence stop
2	TURC0	L = Char. count to AAB 01
3	TURC5	H = Counter reset
4	CSG 22	L = Clocks sequence stop
5	CUF 10	H = Cursor enable
6	CUF 00	L = Cursor enable
7	TURL3	H = Char. count to AAB 04
8	CDR	L = Character bit 3 set
9	CDR	L = Character bit 2 set
10	CDR	L = Character bit 1 set
11	CDR	L = Character bit 0 set
12	H Blank	H = Unblank
13	CUR 03	H = Cursor enable even
14	CUR 01	H = Cursor enable odd

H High (+)
L Low (0 volts)

Memory Electronics Slot 10

TB 1

Pin	Signal	Level
1		
2		
3		
4		
5		
6		
7		
8	Inhibit	H = Enable Inhibit
9	CRG 00	H = Mem. Data Strobe
10		L = Reset MDSA Flops
11	Read A	H = Read Y Lines
12	Read B	H = Read X Lines
13	Write A	H = Enable Y Drive
14	Write B	H = Enable X Drive

I/O Controller Test Points

The Keyboard Controller has one test block associated with it. The block is designated TB 29 and as previously described, the location is the 29th dual in line logic socket which, for this circuit board, is the last one toward the top of the board.

TB 29

Pin	Signal	Level
1	INF 01*	H = Not R I/O Ready
2		
3		
4	INTGCL	L = Int. Flop Clock Rate
5	READY	H = Ready INT SEL enable
6	ACG BOT	L = Keyboard boot ACK enable
7		
8	ACG W I/O	L = Write I/O ACK enable

TB 29 (Cont.)

Pin	Signal	Level
9	BODKB	L = Keyboard Boot keys
10	ACGT I/O	L = Test I/O ACK enable
11		
12		
13		
14	ACGR I/O	L = Read I/O ACK enable

ASYNCHRONOUS COMMUNICATIONS CONTROLLER

TB 69

Pin	Signal	Level
1	WRT INH	H = Read
2	1 ZERO R	H = 1st zero detect Ready Set
3	OCT 9	Bit time 9 Ready Reset
4	FLIP FLOP M35	H = ACK sent
5	INT SEL IN	H = SEL INT flop set
6	DC 3	Data Clock 3
7	DCK 3	Data Set Clock
8	PARITY	Optioned Bit Count Check
9	DCI*	Data Clock 1 Inverted
10	C I/O	H = Unmask
11	WRT FF	H = Set Write Flop
12	RDY FF	H = Set Ready Flop
13	SD 1	Serial Data In
14	DC 1	Data Clock 1

SYNCHRONOUS COMMUNICATION CONTROLLER

The Synchronous Controller test points are provided in the form of 16 pin test blocks.

TB 42

Pin	Signal	Level
1		
2		
3	Func Decode and W I/O Enable	L
4	ACK	H = I/O ACK Enable
5		
6		
7		
8	S Clock	L
9	Sync Code Bit Counter	
10		
11	Sync Code	
12	S Clock A	H = Clock Bit Ct 1.
13	Sync Code Det	
14	XMT Ready	H
15		
16		

TB 43

Pin	Signal	Level
1	STRB AB	H = Register Strobe
2	INT FLOP	H = INTK
3	CLR SYM	L = Clear
4	READY FLOP	H = Data Ready
5	MASK FLOP	H = MSK Interrupt
6		H = Write
7	R/W FLOP	
8	SYNC CODE	
9		
10		
11		

TB 43 (Cont.)

Pin	Signal	Level
12		
13	TIMING	L
14	SDO	L = Serial Data Out Enable
15		
16		

SPLIT SCREEN CONTROLLER

The Split Screen Controller has one 14-pin test block, TB 10.

TB 10

Pin	Signal	Level
1		
2		
3		
4	TVS9 07	L = Non Interlace A Flop Set
5	VSG 07	L = Set A V Sync Flop
6		
7	GROUND	L
8	VSCLR1	L = Clear V Sync A Flop
9	VSCLR3	L = Clear V Sync B Flop
10	SURL0	H = Line Count Bit 0
11	SURL3	H = Line Count Bit 3
12	SURL1	H = Line Count Bit 1
13	SURL4	H = Line Count Bit 4
14	SURL2	H = Line Count Bit 2

BOOT CONTROLLER TEST POINTS

TB 35

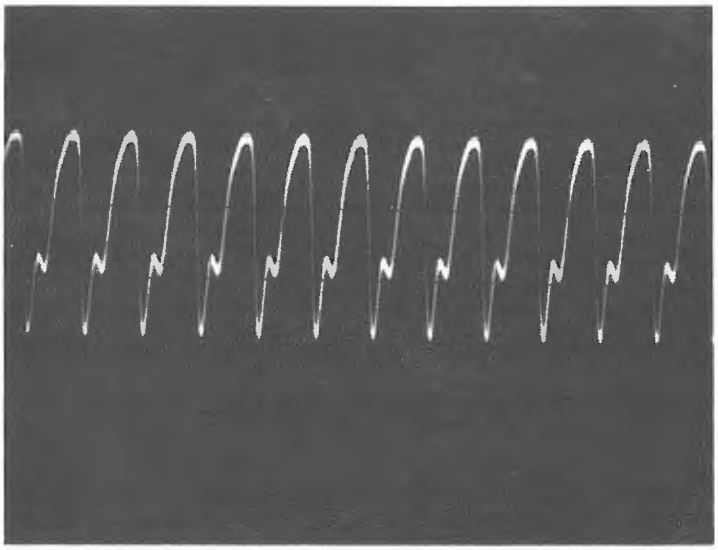
Pin	Signal	Level
1	BOOT 1	Boot Count 1
2	TIME	L = Timer Reset
3	PWIRES	L = Power Reset
4	BOOT A	H = Controller Boot
5	CALPHA	H = Character Available
6	BOCHCG	L = Boot Detect
7	CADCG	H = Carrier Detect
8	BOOT A RES	L = Reset Boot Count
9	BOOT RES	L = Boot Count Reset
10	BODRF	L = Boot Disable
11	EBGBOT	L = Error Boot A Reset
12	BOOT 2	Boot Count 2
13	ADD1/GEN	H = Address 1 General Character Count
14	ADD1/GENRE	L = Boot Count Reset

7.5 WAVEFORMS

The following waveform photographs were taken from the scope face of a Tektronix 422 oscilloscope. The SPD 10/20 terminal contained an operating program and all probe points were accessed with only the top cover removed from the terminal.

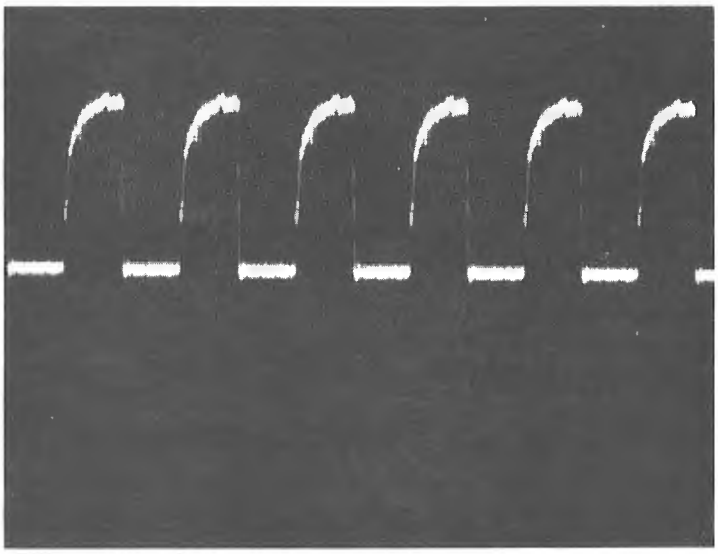
WARNING

Removal of the top cover from the SPD 10/20 Display terminal exposes hazardous voltages and should only be performed by qualified personnel.



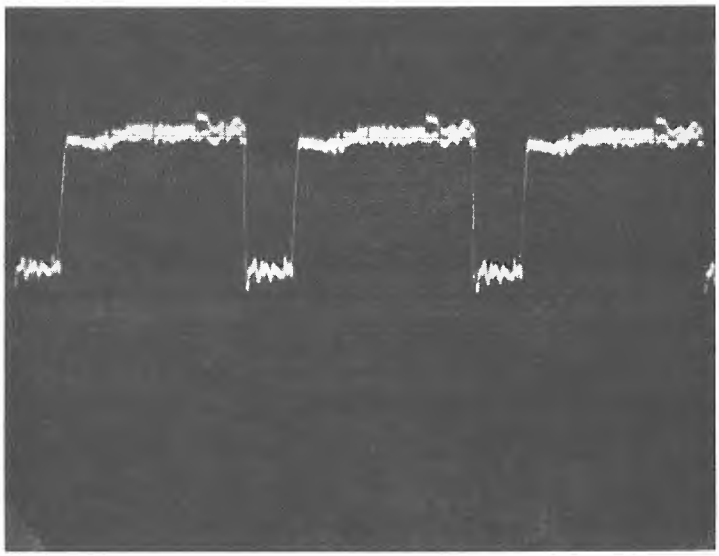
Location: Pin 1 M106 RMTU
Volts/Div: 0.2 x 10
Time/Div: 0.1 microseconds

LINE LOCK 12.6 MHz



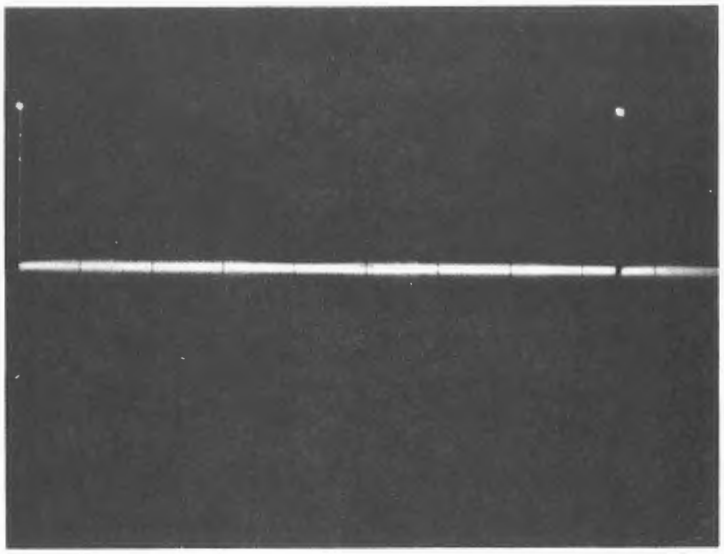
Location: Pin 12 M108 RMTU
Volts/Div: 0.2 x 0
Time/Div: 1.0 microseconds

TURT 4



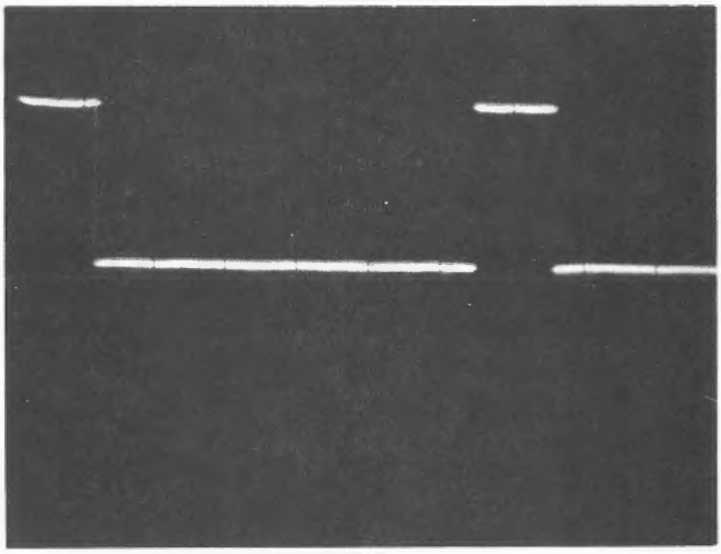
Location: Pin 1 M40 RMTU
Volts/Div: 0.2 x 10
Time/Div: 0.5 microseconds

CRG 00



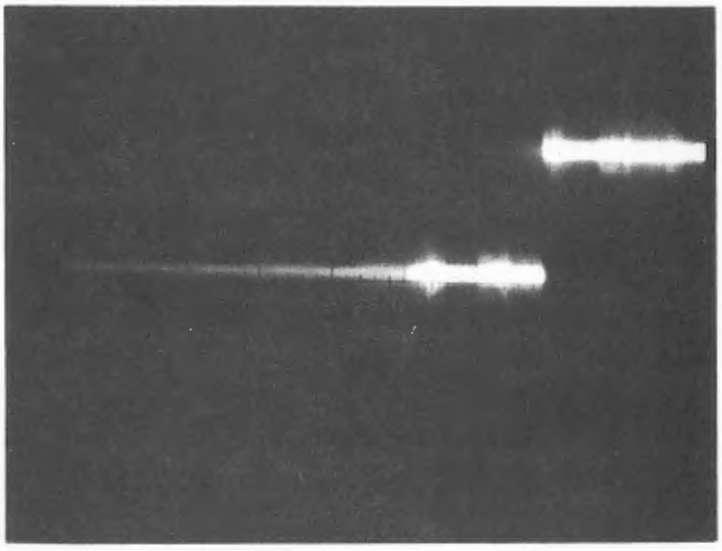
V SYNC

Location: Pin 8 M20 RMTU
Volts/Div: 0.2 x 10
Time/Div: 2.0 milliseconds



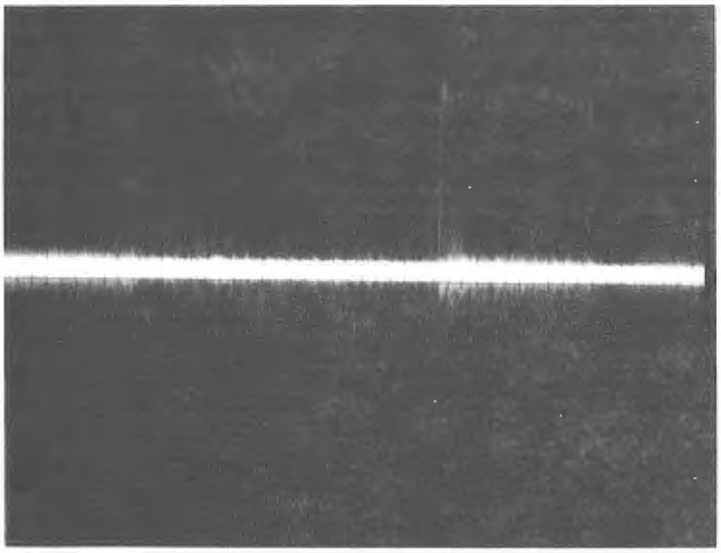
H SYNC

Location: Pin 6 M20 RMTU
Volts/Div: 0.2 x 10
Time/Div: 10 microseconds



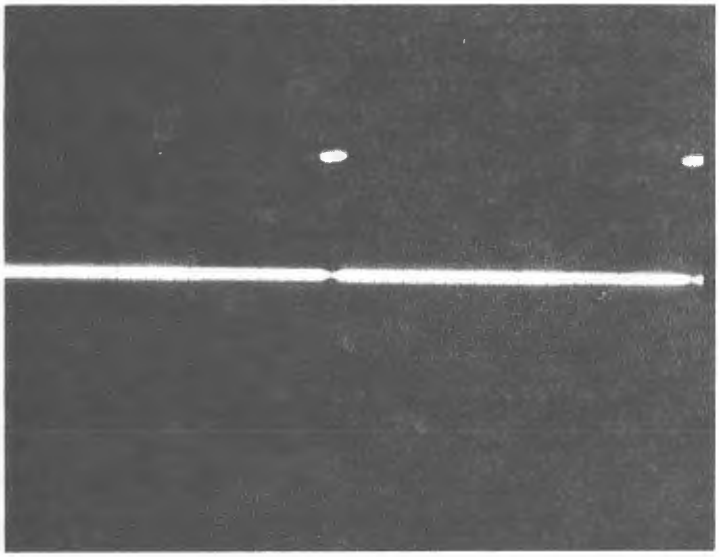
RTC

Location: Pin 12 M94 RMTU
Volts/Div: 0.2 x 10
Time/Div: 5 milliseconds



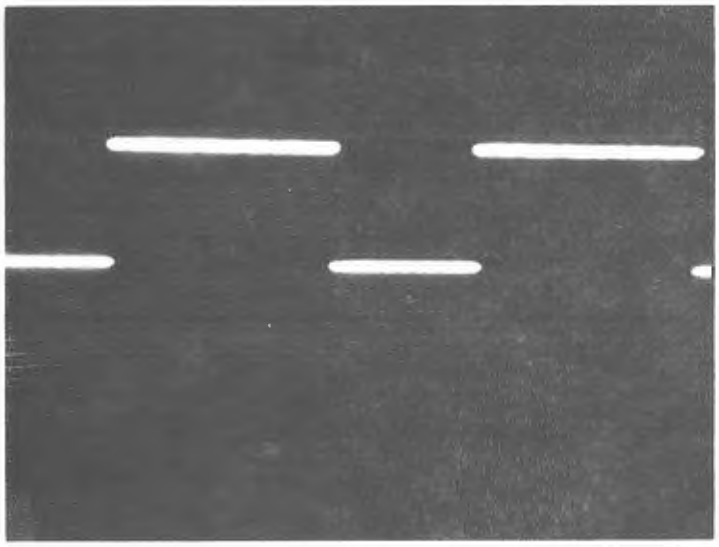
VIDEO

Location: Pin 8 M7 RMTU
Volts/Div: 0.2 x 10
Time/Div: 10 microseconds



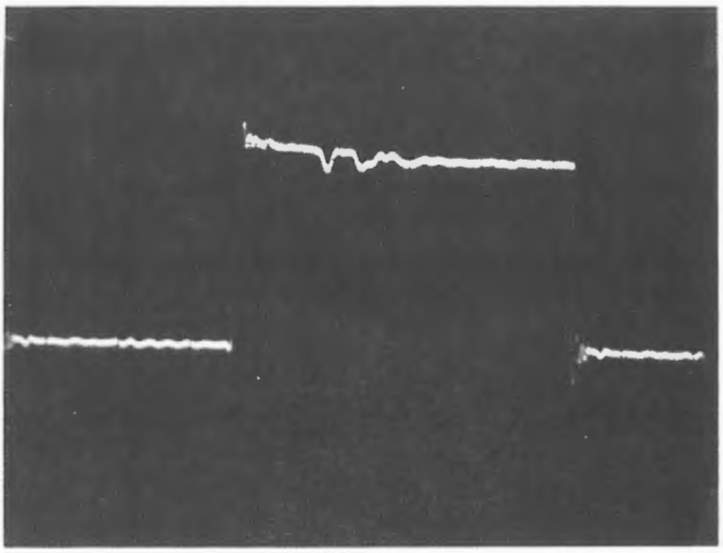
REF REQ

Location: Pin 15 M45 RMTU
Volts/Div: 0.2 x 10
Time/Div: 0.1 milliseconds



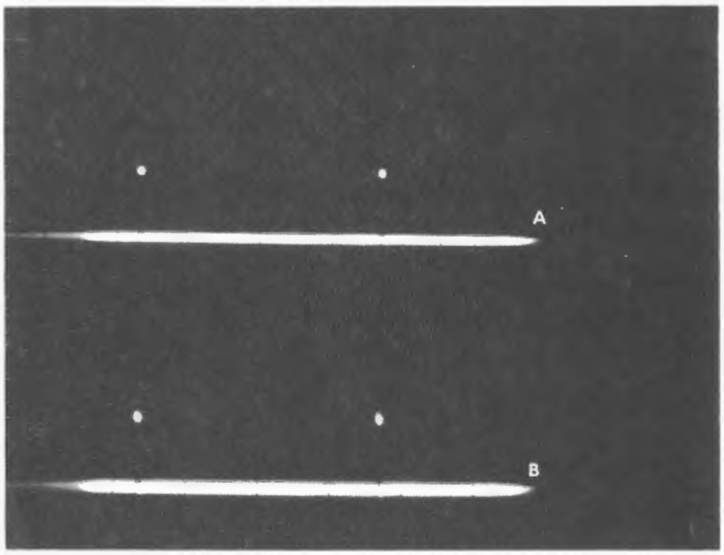
REF SIG

Location: Pin 11 M45 RMTU
Volts/Div: 0.2 x 10
Time/Div: 0.1 milliseconds



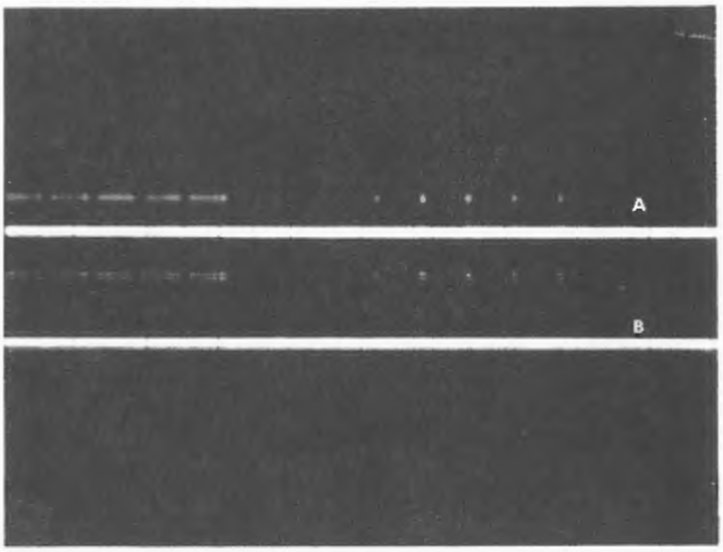
Location: Collector of inhibit transistor MEL
Volts/Div: 0.5 x 10
Time/Div: 0.2 microseconds

I inhibit collector of transistor BIT 16



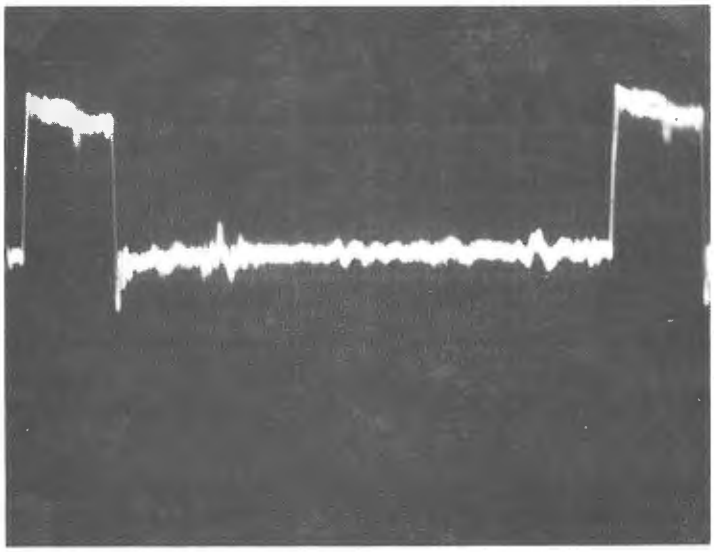
Location: Pins 6 & 8 M18 Split Screen
Volts/Div: A 0.5 x 10
B 0.5 x 10
Time/Div: A & B 5 milliseconds

SPLIT SCREEN V SYNC



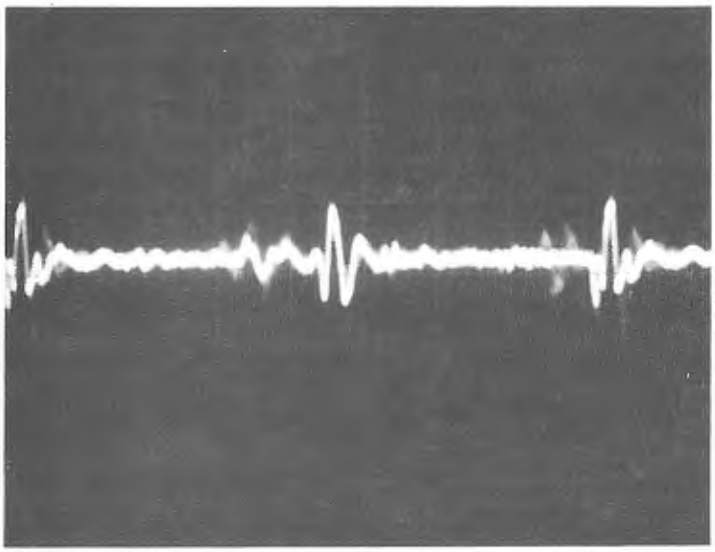
Location: Pins 6 & 8 M13 Split Screen
Volts/Div: A 0.5 x 10
B 0.5 x 10
Time/Div: 0.1 milliseconds

SPLIT SCREEN VIDEO



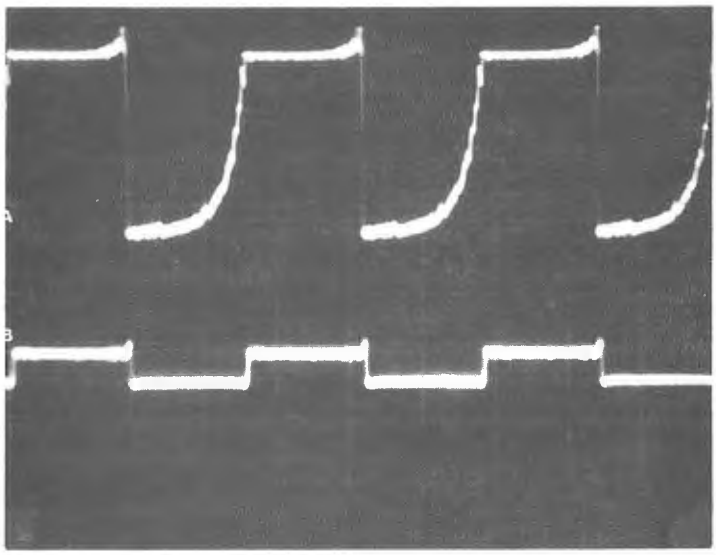
MEM DATA SENSE AMP STROBE

Location: Pin 10 E9
Mem Stack
Volts/Div: 0.2 x 10
Time/Div: 0.2 microseconds



M DATA SENSE AMP OUTPUT

Location: Pin 12 E8
Mem Stack
Volts/Div: 0.2 x 10
Time/Div: 0.2 microseconds



A-INT SEL IN B-INT SEL OUT
Keyboard Controller

Location: A Pin 3 M18 KB
B Pin 8 M11 KB
Volts/Div: A 0.5 x 10
B 0.2 x 10
Time/Div: 0.5 microseconds

7.6 CRT ADJUSTMENTS

Several adjustments are provided on the monitor chassis to provide image clarity, vertical and horizontal picture stability and character size. The cover must be removed from the Terminal to expose the adjustment controls.

> **CAUTION**
>
> No work should be attempted on an exposed monitor chassis by anyone not familiar with servicing procedures and precautions.

All adjustments except centering and focus are shown in Figure 7-6. Centering and focus adjustments are shown in Figure 7-7.

The adjustments are listed below:

Voltage Regulator Adjustment - Connect a voltmeter between the bottom of the capacitor and chassis ground. Adjust potentiometer for a meter reading of 24 volts.

Horizontal Linearity - This adjustment requires positioning of a slug with a tuning wand. Observe right side of picture and adjust CCW for maximum width.

Width - This adjustment also requires positioning of a slug with a tuning wand. Adjust raster width to 8-1/2 inches.

Horizontal Trimmer - This adjustment is on the bottom PC board. Set the Horizontal Hold adjustment for the most left position then adjust the trimmer to position the left character at the edge of the raster.

Centering Tabs - Position the tabs opposite one another then adjust as required to obtain a centered condition.

Focus Tabs - Position the tabs opposite one another then adjust as required to obtain proper focus.

There are five adjustments on the top of the chassis that can be used for fine adjustment of the CRT for clarity and stability. They are shown in Figure 7-6 and are identified as follows:

Vertical Hold	Vertical Linearity	Vertical Height
Horizontal Hold	Contrast	

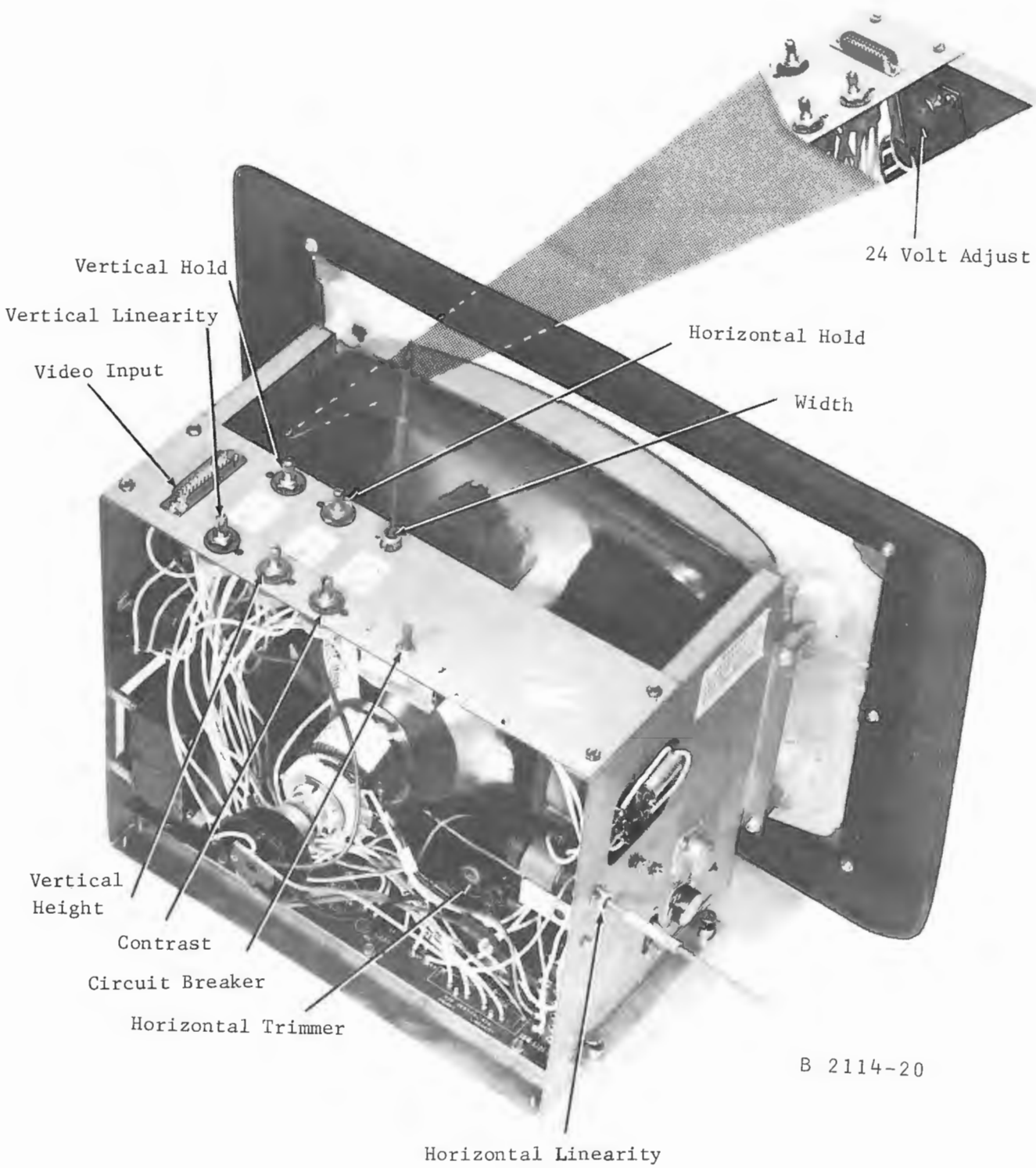


Figure 7-6. T. V. Monitor Adjustments

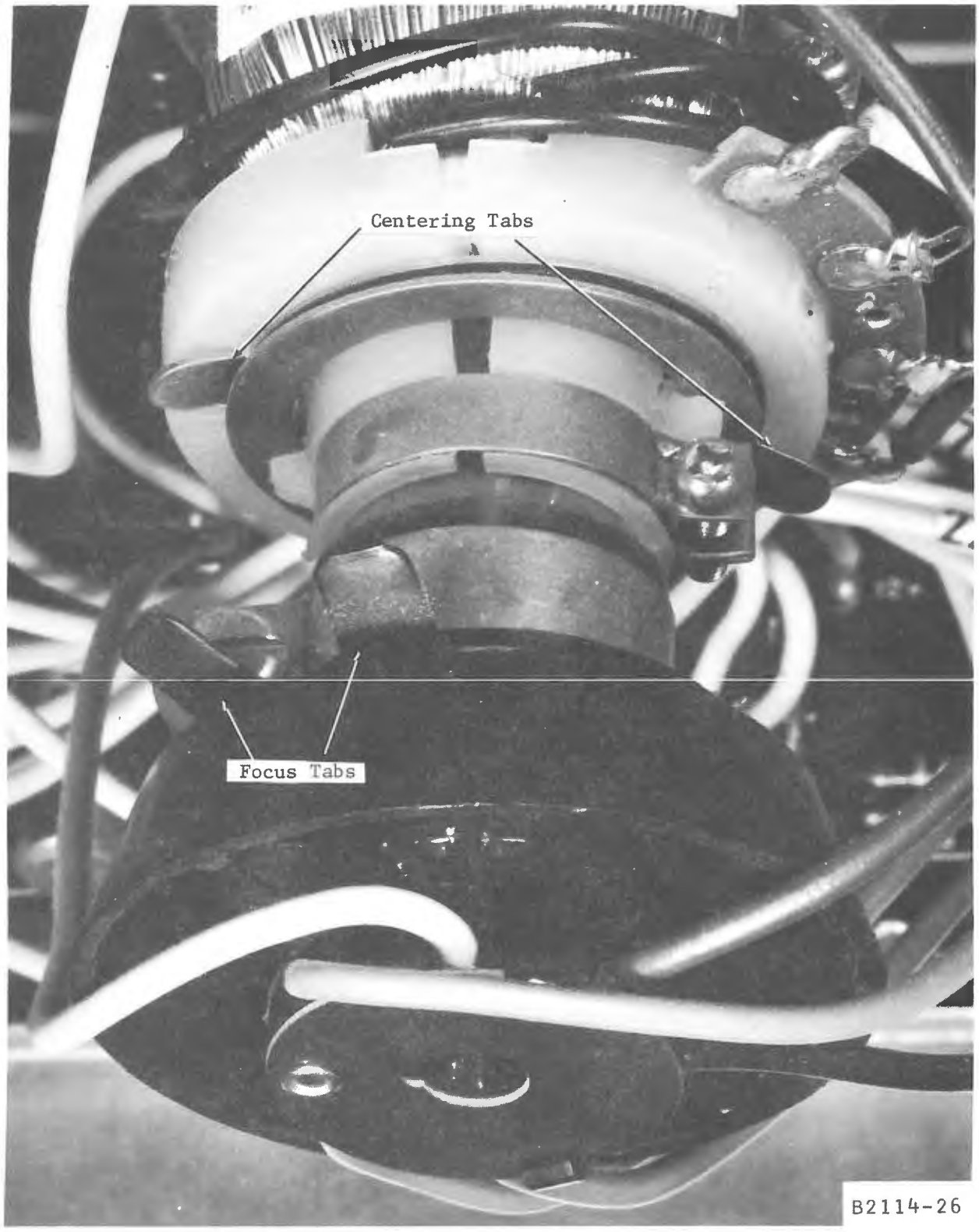


Figure 7-7. Cathode Ray Tube Adjustments

APPENDIX A

SIGNAL GLOSSARY

A. 1 The following list of signals has been derived from the back plane wiring list for the computer circuitry (large plane) Print 005-10-30 Rev B.

Mnemonic	Description and Definition
AAB 00-11	Auxiliary Arithmetic Bus, Bits 0 through 11. The AAB is a 12-bit low truth bus which provides a data path from various system data registers to the Auxiliary Arithmetic Unit address.
AAR/AAU	This signal indicates a data transfer from the Auxiliary Arithmetic Register to the Auxiliary Arithmetic Unit.
AAR/CUR	This signal indicates a data transfer from the Auxiliary Arithmetic Register to the Cursor Register. The CUR, composed of the 6-bit Line and Character Registers taken together, for a total of 12 bits.
AAR/MAB	This signal indicates a data transfer from the Auxiliary Arithmetic Register to the Memory Address Bus. The MAB is a low truth, 12-bit bus.
AAR/MDB	This signal indicates a data transfer from the Auxiliary Arithmetic Register to the Memory Data Bus. The MDB is a low truth, 16-bit bus.

Mnemonic	Description and Definition
AAU/CSR	This signal indicates a data transfer from the Auxiliary Arithmetic Unit to the Condition Status Register. The CSR is a 3-bit register.
ACR/ARB	This signal indicates a data transfer from the Accumulator to the Arithmetic Bus. The ARB is a 7-bit, high truth bus.
ACR/ARU	This signal indicates a data transfer from the Accumulator to the Arithmetic Unit. The ARU is an 8-bit, logical adder.
ACR K IN	The Accumulator is an 8-bit device. This signal is a steering signal for ANDing or ORing Accumulator data with MDR data. The K input enables ORing.
ACR J IN	As the last signal indicated, the J enables the ANDing.
ACR/MDB	This signal indicates a data transfer from the Accumulator to the Memory Data Bus. The MDB is a 16-bit, low truth bus.
ARB 00 through 07	These signals provide the actual digital weighted value (positioned) for data on the Arithmetic Bus.
CC G 56	This signal originates on the RMTU at a character code gate.
CPI	This designation stands for clock pulse inverted.
CPI 11	There are a series of clock pulse inversions within the system. The numbers following the I indicate phases (of the 20) are present. The one illustrated is 11, which means phase 1 or 11. Others are CPI 22 2 or 12, etc.
CPT	Again this is a true clock (no inversion).
CPT 02	The numbers following the letter designation indicate which phase of the 20 phase clock system is the signal applied to.

Mnemonic	Description and Definition
CRG 00	This is an RMTU derivative of the basic timing used as a strobe in the core memory sense amplifiers.
CUR/AAB	This signal indicates a data transfer from the Cursor Register to the Auxiliary Arithmetic Bus.
EXT F1	This is a state of the Auto Exec. cycle.
EXT W	Same as EXT F1.
FUN 00 through 03	These 4 bits are programmed in I/O instructions to provide various functions for controller operation associated with the TYPE code.
IO/ARB	This signal enables the IO Bus to the Arithmetic Bus.
I0A through 15A (Z0 through Z15)	These 16 signals are the respective bit inhibit currents.
LOW/AAB	This signal is used in memory top sector determination.
LOW/ARB M	This signal is used in the boot state.
MAB	Memory Address Bus. The MAB is a 12-bit, low truth bus.
MAB SP 00 through 11	These 12 bits are for special address access to the MAB. These are the only signals which get to the MAB directly. The other (normal) path is through the AAR (Auxiliary Arithmetic Register).
MAR 00 through 11	This is the 12-bit register which accesses core for the purpose of addressing. The MAR can also be enabled to the AAB for address manipulation.
MAR*	This is the not side of a memory address bit register. The asterisk is used to indicate the not sometime illustrated as a horizontal bar, example: $\overline{\text{MAR}}$.
MAR/CUR	This signal indicated a data transfer from the Memory Address Register to the Cursor Register (Line and Character combined).

Mnemonic	Description and Definition
MAR/AAB	This signal indicates a data transfer from the Memory Address Register to the Auxiliary Arithmetic bus.
MDR/AAB	This signal indicates a data transfer from the Memory Data Register to the Auxiliary Arithmetic Bus.
MDR/ARB	This signal indicates a data transfer from the Memory Data Register to the Arithmetic Bus.
MDB CM 00 through 15	These 16 bits are one complete core memory word which can be strobed from the core memory to the Memory Data Bus.
MDR 00* through 15*	The asterisk indicates the signal is the not of a memory data bit.
MDSA 0 through 15	These signals are a complete 16-bit memory word detected at individual sense amplifiers.
MEM STROBE	This is an enabling signal used to strobe data into or out of data registers or actual core registers.
OPDG	This signal is indicative of a group of signals which are decoded operating commands.
OTB 00 through 04	This signal comprises the lower four bits on the output bus.
PCR/ARB	This signal indicates a data transfer from the Program Counter Register to the Arithmetic Bus.
PWR UP	This signal when true, indicates the proper operating voltage is present. The system is electronically interlocked such that a loss of power creates an ordered power down procedure and prevents memory from being lost.
REFREQ	This signal is found in the refresh circuitry and indicates the frequency of refresh.

Mnemonic	Description and Definition
REFSIG	This is the actual data being refreshed.
RESET	Reset signals are found throughout the terminal. The use of the reset signal is generally to return a flip flop or group of flip flops back to a known condition after a particular function has been completed.
RM AAB	This signal is the enabling of the Refresh Area of memory to the Auxiliary Arithmetic Bus.
RTC	Real Time Clock. The RTC provides the capability of performing various control functions in the realm of real time as opposed to system time. The clock itself is free running at 15 Hz rate.
STRB AAR	Similar to MEM STROBE. The signal is a data enabler to the Auxiliary Arithmetic Bus.
STRB ACR L	This signal strobes the four least significant bits in the Accumulator.
STRB ACR M	This signal strobes the four most significant bits in the Accumulator.
STRB BYTE	This signal indicates the enabling of a byte's worth of data which is eight bits.
STRB CHR	This signal enables the strobing of data from the Character Register. The CHR is a 6-bit register.
STRB CSR	This strobe is for the Condition Status Register, a 3-bit register which sets with the results of arithmetic operations.
STRB LIR	This is a strobe for Line Register data. The LIR is a 6-bit register.
STRB MAR	This strobe is for memory address data.
STRB MDR	This strobe is for memory data.
STRB PCR	This strobe is for Program Counter data.

Mnemonic	Description and Definition
TOP SEC	This signal becomes true when the addressed word in memory is programmed to be the top sector of memory. It is the signal that causes the Memory Address Register to direct the data to the right area (sector) of memory.
TUD	This signal is a timing unit decode.
TURL 0 through 4	This signal identifies the four-bit register used for line count timing. Timing Unit Register Line zero through four.
TURT 4	This signal is a clock signal from the RMTU which is always present. It stands for Timing Unit Register time 4.
WAIT	Wait is a programmed processor mode. In this mode, the processor is waiting for data to operate on.
XND 0 through 3	These four signals indicate the memory X axis current direction. In this case it is ND = Negative direction.
XPD 0 through 3	The positive direction of X current.
XR 0 through 7	This is the memory X axis source or sink, depending on whether in the Read or Write mode.
YND 0 through 7	Same as XND except it is for the Y axis.
YPD 0 through 7	Same as YND 0 through 7.
YR 0 through 7	Same as XR, except for the Y axis.
+1 AAU	This signal indicates the data in the Auxiliary Arithmetic Unit will have +1 added to it. This is an increment instruction.
-1 AAU	Same as above occurring as a decrement instruction.
+2 AAU	Same as +1.
+4 AAU	Same as +1.

A. 2 The following signals are used on I/O controller schematics and in I/O wiring diagram 005-10-28.

Mnemonic	Description and Definition
ACK	This signal is a controller response to the TPU TYPE and function commands. TPU ACK indicates the controller state of readiness.
AKD RTC	Real Time Clock signal.
ATTENTION	This signal indicates that an I/O instruction is in progress. It may or may not be used.
BOOT	This signal indicates the TPU mode of operation. When BOOT is enabled, no other device may be serviced. This signal is associated with program loading either local or remote.
CONT 00 through 07	This signal is an addressing line wired to each I/O slot in the TPU.
CPT (RET)	This signal is physically located in a twisted pair. It is the return line for a clock pulse.
INB 00 through 07	The eight bits of input data on the I/O bus.
INT 0 through 7	The signals are wired to each I/O controller Circuit Board Connector. The interrupt line is a part of the dedicated system to determine which device is presenting or requesting data.
INT SEL IN	This is the interrupt selected input signal from the TPU. The interrupt select is passed from controller to controller until a controller requests service at which time the INT SEL IN is stopped.
INT SEL OUT	This signal is sent to the TPU from a controller which has responded to the above signal and is ready to give or receive data.

Mnemonic	Description and Definition
TYPE 00 through 01	This two-bit programmed signal (bits 8 and 9) is fed to the various controllers under the four possible conditions of: 00 TIO (Test) 01 CIO (Control) 00 RIO (Read) 11 WIO (Write)

APPENDIX B

OPTION BLOCKS

B.1 GENERAL

The SPD 10/20 Terminal Processing System has been designed with built-in communication versatility. This versatility is provided in the form of option blocks located on various circuit boards within the system. The option block scheme provides the customer with a wide choice of system operation in his application. Most options selectable in the area of input/output circuitry are provided to allow compatible operation within the various data communications schemes used within the industry. Optional operating modes can affect the transmitted and received data word length, start and stop codes, sync codes, and speed of data transfer or Baud rate. Within the Terminal processor, options include I/O interrupt assignment selection, memory option, selection of the blink bit and other functions. Since a large number of possible options exist, this Appendix graphically presents those known, along with the part number, subassembly used, and function.

B.2 STB LOCATION

The location of a particular option block is provided in the form of an STB number. The STB number in most cases can be counted up to by holding the circuit board with components facing you and counting the TTL elements from the bottom row, left to right (the async controller has the number etched on the board). After counting a row, return to the left, go

up one row, and repeat until reaching number desired. The only time this does not work is on the Series 001 control board, where only the STB positions are counted. The 005 board follows the normal counting sequence. The circuit board photographs contained in Chapter V and VI locate the various STB positions.

B.3 PART NUMBER

The first five digits of the part number are identical for either the 16-pin or 32-pin option block. The next two digits (01, 02) designate the 16-pin (01) and 32-pin (02). The final 700 series number is the distinct wiring configuration for each option.

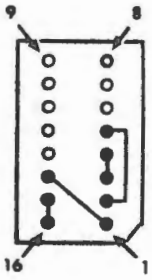
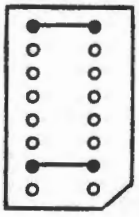
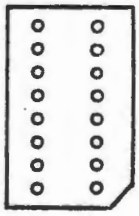
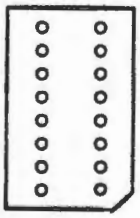
B.4 CONVENTIONS USED

The Real Time Clock is permanently wired on the Control Board to be Address 15. The RMTU can be selected, but generally is address 8. Address 00 should be avoided because an I/O Read or Write issued to a non-existent controller will cause a loss of data. Since uniformity of program application results if various programs conform to a set format, the following guide is commonly used.

Controller Slot	Function	Address
C1	Master Keyboard	2
C2	Synchronous/Asynchronous	2
C3	Slave Keyboard	3
C4	Boot Controller	not assigned
C5	Printer Controller	5
RMTU	Refresh Control	8
J9	Program Loader	1
RTC	Real Time Clock	15 (Hard wired)

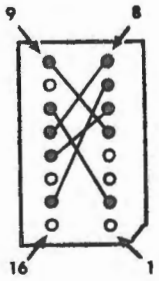
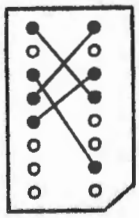
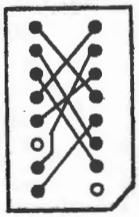
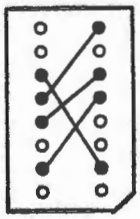
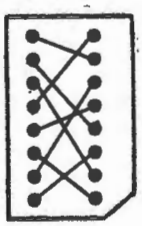
The remainder of this appendix is devoted to a presentation of all known option blocks as of this publication date. Throughout the listing unused blocks are left in for possible future additions.

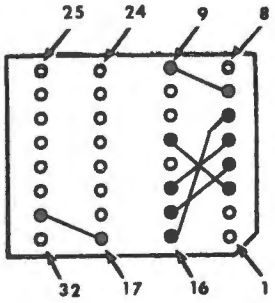
B.5 TPU DATA FLOW

	Part NO.	STB NO.	Function
	001-11-01-701	114	2K Memory Option
	001-11-01-713	63*	
			
			

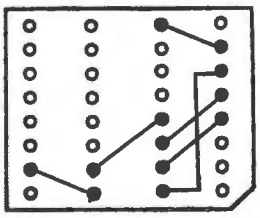
*Insert pin 1 of Block in pin 1 of receptacle, use on 006 only.

B.6 TPU CONTROL

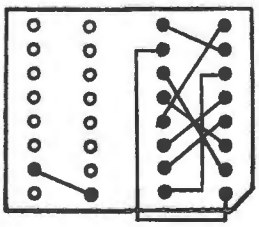
	Part NO.	STB NO.	Function
	001-11-01-702	1 (001 board) 4 (005 board)	CCN Option
	001-11-01-718	1 (001) 4 (005)	C1 - INT 2 C2 - INT 4 C3 - INT 3 J 9 - INT 1
	001-11-01-745	1 (001) 4 (005)	C1 - INT 2 C2 - INT 4 C3 - INT 3 C5 - INT 5 C6 - INT 6 C8 - INT 7 J 9 - INT 1
	001-11-01-746	1 (001) 4 (005)	C1 - INT 2 C2 - INT 4 C3 - INT 5 J 9 - INT 1
	001-11-01-782	4	C1 - INT 2 C2 - INT 5 C3 - INT 4 C5 - INT 3 C6 - INT 7 C7 - INT 6 C8 - INT 0 J 9 - INT 1



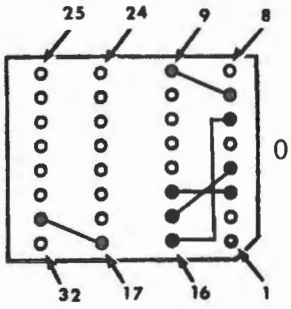
Part NO.	STB NO.	Function
001-11-02-701	2 and 3 (001) 13 and 14 (005)	CCN Option



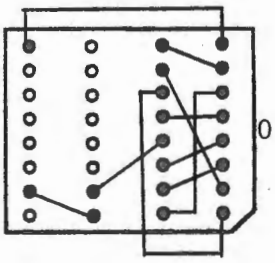
001-11-02-708	2 and 3 (001) 13 and 14 (005)	C1 - ADD 2 C2 - ADD 4 C3 - ADD 3 C4 - ADD 9 J9 - ADD 1 RMTU - ADD 8



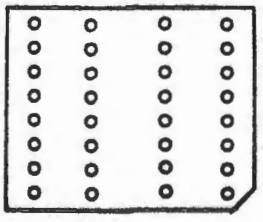
001-11-02-718	2 and 3 (001) 13 and 14 (005)	C1 - ADD 2 C2 - ADD 4 C3 - ADD 3 C4 - ADD 4 C5 - ADD 5 C6 - ADD 6 C8 - ADD 7 J9 - ADD 1 RMTU - ADD 8



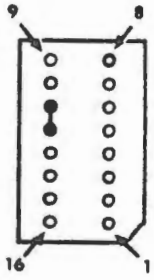
Part NO.	STB NO.	Function
001-11-02-719	2 and 3 (001) 13 and 14 (005)	C1 - ADD 2 C2 - ADD 4 C3 - ADD 5 J 9 - ADD 1 RMTU - ADD 8



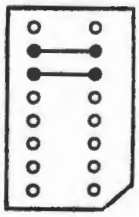
001-11-02-724	13 and 14	C1 - ADD 2 C2 - ADD 5 C3 - ADD 4 C4 - ADD 9 C5 - ADD 3 C7 - ADD 6 C8 - ADD 0 RMTU - ADD 8 RTC - ADD 15 J 9 - ADD 1 C6 - ADD 7



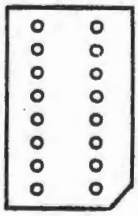
B.7 MEMORY ELECTRONICS

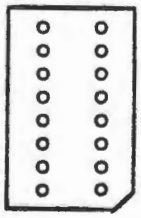


Part NO.	STB NO.	Function
001-11-01-711	41	1K Memory Option

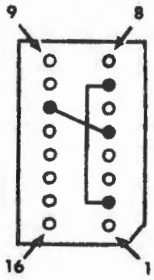
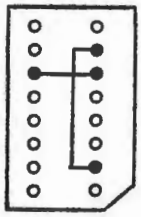
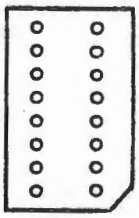
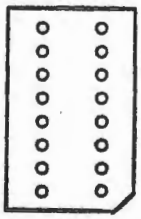


001-11-01-712	41	2K Memory Option

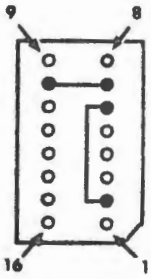
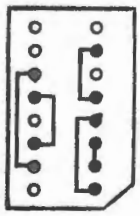
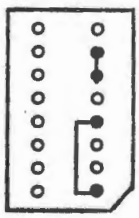
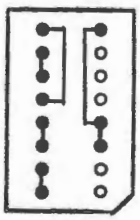


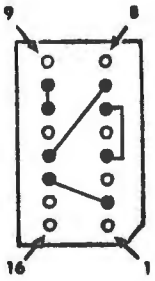


B.8 REFRESH MODULE TIMING UNIT

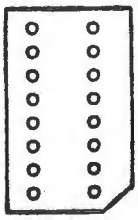
	Part NO.	STB NO.	Function
	001-11-01-701	105	Clock Enable Decode for Blink
	001-11-01-710	105	8th Bit Character Blink
			
			

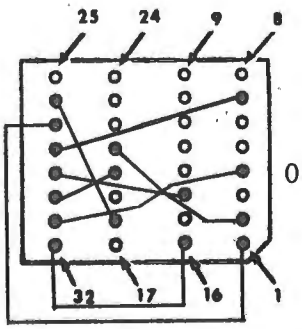
B. 9 SYNCHRONOUS CONTROLLER

	Part NO.	STB NO.	Function
	001-11-01-705	54	CCN Board 001-08-02-701 Rev B
	001-11-01-706	51	CCN Board 001-08-02-701 Rev B
	001-11-01-707	48	CCN Board 001-08-02-701 Rev B
	001-11-01-708	52	CCN Board 001-08-02-701 Rev C and up.



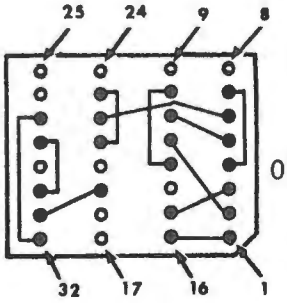
Part NO.	STB NO.	Function
001-11-01-709	28	CCN Board 001-08-02-701 Rev C and up.



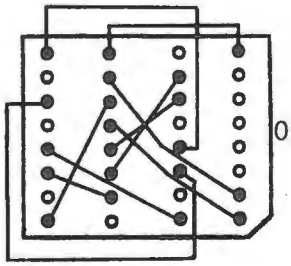


001-11-02-702	15 and 16	CCN Board 001-08-02-701 Rev B

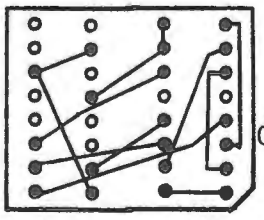
B. 9 SYNCHRONOUS CONTROLLER (Cont.)



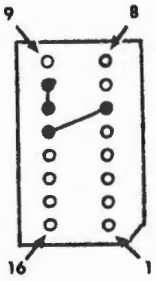
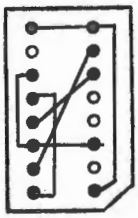
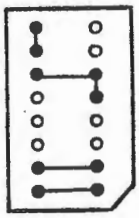
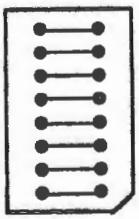
Part NO.	STB NO.	Function
001-11-02-703	18 and 19	CCN Board 001-08-02-701 Rev B

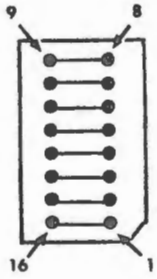
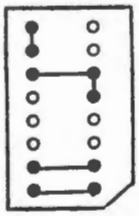
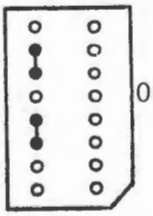
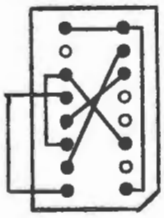


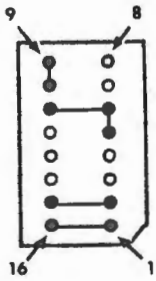
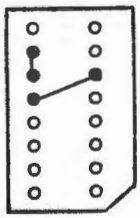
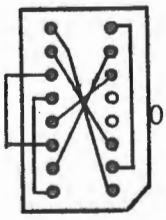
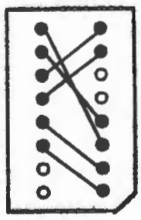
001-11-02-704	15 and 16	CCN Board 001-08-02-701 Rev C and up.



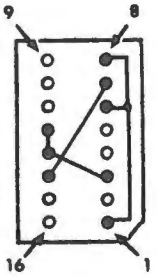
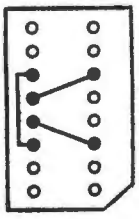
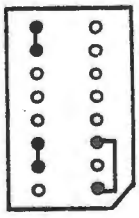
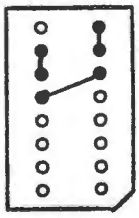
001-11-02-705	22 and 23	CCN Board 001-08-02-701 Rev C and up.

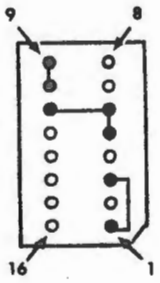
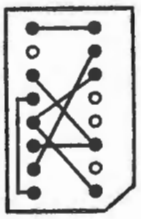
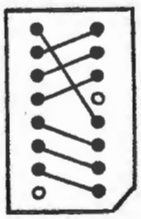
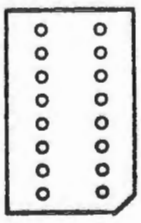
	Part NO.	STB NO.	Function
	001-11-01-714	42	Multiplexer Option (Same as 727)
	001-11-01-715	67	Word Length 10 Bits (Same as 722)
	001-11-01-716	26	Data Set Inputs (Same as 726)
	001-11-01-717	12	8 Bit Data for Receive Mode

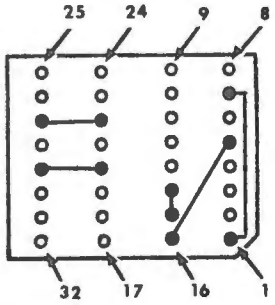
	Part NO.	STB NO.	Function
	001-11-01-719	26	Data Set Connections
	001-11-01-720	12	8 Bit Data for Receive
	001-11-01-721	42	External STC Clock from Multiplexer
	001-11-01-722	67	10 Bit Data (1 Start, 8 Data, 1 Stop)

	Part NO.	STB NO.	Function
	001-11-01-726	26	Data Set Connections. Complete Option Blocks for ASYNC to Printer (STB 12 Not Needed)
	001-11-01-727	42	Multiplexer Connections for straight async.
	001-11-01-728	67	Word Length 11 Bit 1 Start 8 Data 2 Stop
	001-11-01-747	12	8 Bit Data 1 Start 6 Data 1 Stop

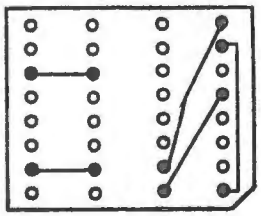
B. 10 ASYNCHRONOUS CONTROLLER (Cont.)

	Part NO.	STB NO.	Function
	001-11-01-748	67	8 Bit Data 1 Start 6 Data 1 Stop
	001-00-01-759	42	Async Data Over Sync Modem. Non- MUX Operation.
	001-11-01-783	26	Full Duplex Receive Only.
	001-11-01-784	42	Internal Clock Non-MUX.

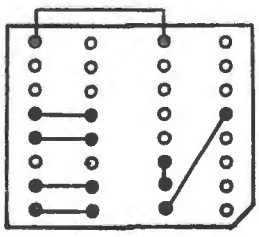
	Part NO.	STB NO.	Function
	001-11-01-785	26	Full Duplex for Transmit
	001-11-01-786	67	9 Bit Word 1 Start 7 Data 1 Stop
	001-11-01-787	12	7 Data Bits
			



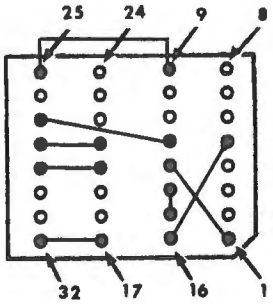
Part NO.	STB NO.	Function
001-11-02-706	65 and 66	1200 Baud Internal Clock, Even Parity Gen. and Check



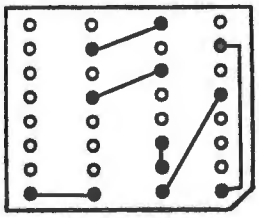
001-11-02-707	65 and 66	2400 Baud Even Parity Check and Gen. External Transmit Clock



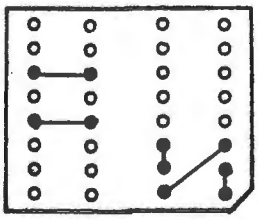
001-11-02-710	65 and 66	330 Baud, Even Parity Gen. Internal Clock



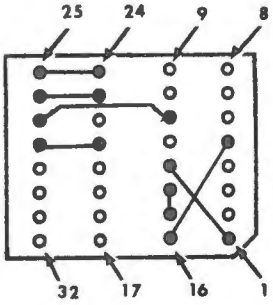
Part NO.	STB NO.	Function
001-11-02-717	65 and 66	110 Baud, 11 Bit Data, Gen. Parity No Parity Check



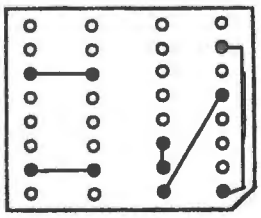
001-11-02-720	65 and 66	200 Baud, Even Parity Check and Gen. Internal Clock



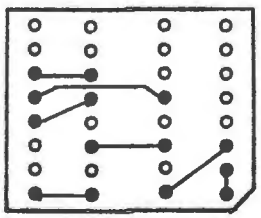
001-11-02-721	65 and 66	1200 Baud, No Parity Internal Clock



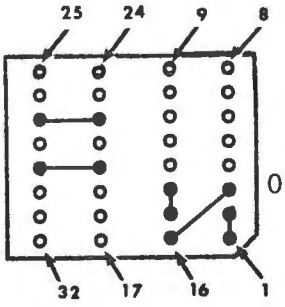
Part NO.	STB NO.	Function
001-11-02-722	65/66	300 Baud Internal Clock, Even Parity Gen. No Parity Check



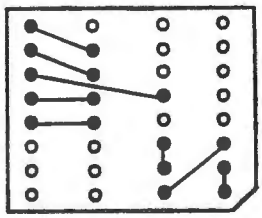
001-11-02-723	65/66	2400 Baud, Even Parity Check and Gen.



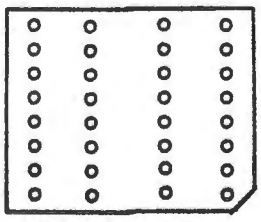
001-11-02-725	65/66	150 Baud Transparent Parity Gen. and Check



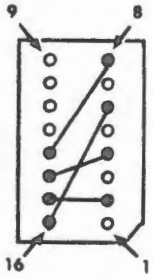
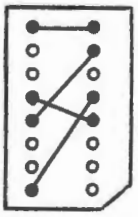
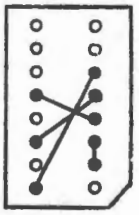
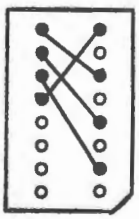
Part NO.	STB NO.	Function
001-11-02-726	65/66	1200 Baud, Transparent Parity Check and Gen.

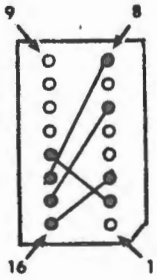
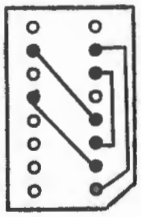
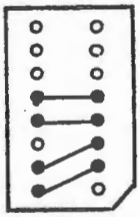
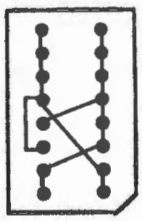


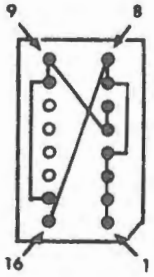
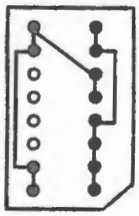
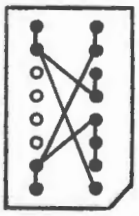
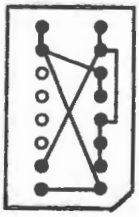
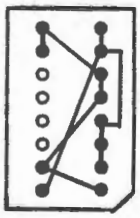
001-11-02-727	65/66	135 Baud Transparent Parity Check and Gen.

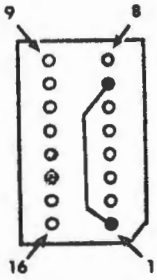
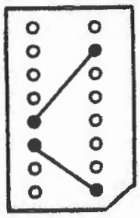
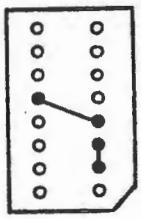
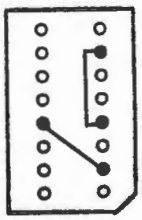


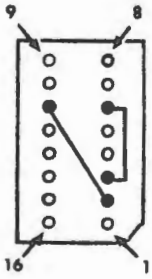
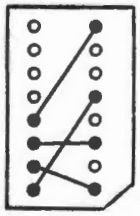
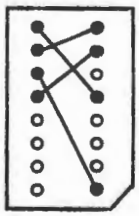
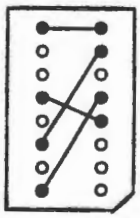
B.11 BOOT CONTROLLER

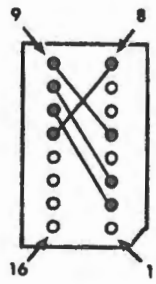
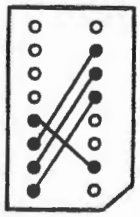
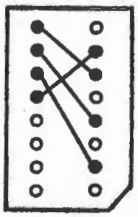
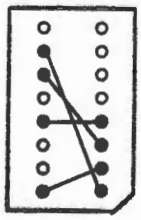
	Part NO.	STB NO.	Function
	001-11-01-729	22	1/2 GEN/ERR Address 0 (hex)
	001-11-01-730	31	1/2 Boot Char C(hex)
	001-11-01-731	49	1/2 Boot Char 9(hex)
	001-11-01-732	29	1/2 ADD 1 2(hex)

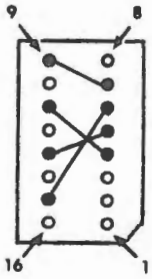
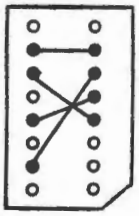
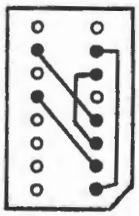
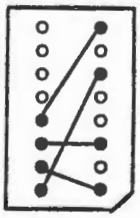
	Part NO.	STB NO.	Function
	001-11-01-733	47	1/2 ADD 1 = C(hex)
	001-11-01-734	19	1/2 GEN/ERR Address = C(hex)
	001-11-01-735	23	Time out = 1 min.
	001-11-01-736	11	R I/O ADD 1 = 42(hex)

	Part NO.	STB NO.	Function
	001-11-01-737	11	R I/O Address 2 = 42(hex)
	001-11-01-738	10	R I/O Address 2 = 43(hex)
	001-11-01-739	10	R I/O Address 2 = 44(hex)
	001-11-01-740	10	R I/O Address 2 = 45(hex)
	001-11-01-741	10	R I/O Address 2 = 46(hex)

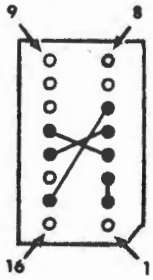
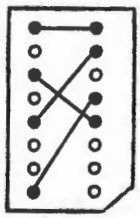
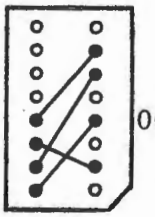
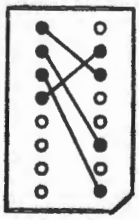
	Part NO.	STB NO.	Function
	001-11-01-750	28	ADD 2 Inhibited
	001-11-01-751	45	4 MSB EDB = XX11
	001-11-01-752	49	4 MSB BOOT Char. = XX01
	001-11-01-753	47	4 MSB ADD 1 = XX01

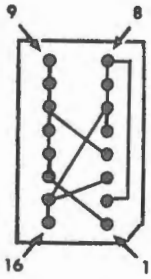
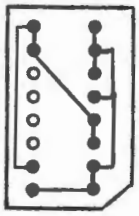
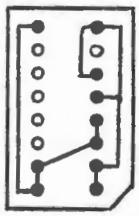
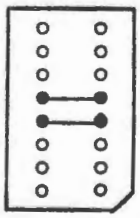
	Part NO.	STB NO.	Function
	001-11-01-754	19	4 MSB ERROR Char = XX01
	001-11-01-755	22	4 LSB ERROR Char = 1110
	001-11-01-756	27	4 LSB EOB = 1101
	001-11-01-757	31	4 LSB Boot Char = 1110

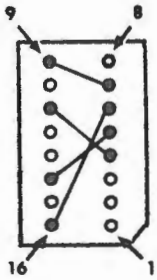
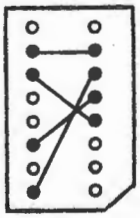
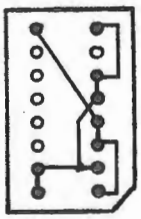
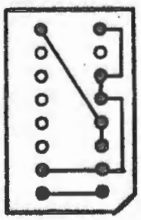
	Part NO.	STB NO.	Function
	001-11-01-758	29	4 LSB ADD 1 Char = 1110
	001-11-01-760	47	MSB ADD 1(hex 5)
	001-11-01-761	29	LSB ADD 1(hex 3)
	001-11-01-762	46	MSB ADD 2(hex 3)

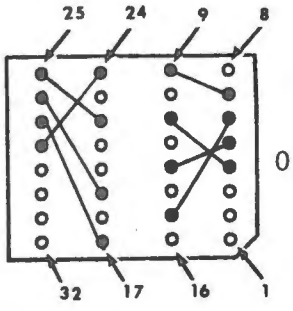
	Part NO.	STB NO.	Function
	001-11-01-763	28	LSB ADD 2(hex 2)
	001-11-01-764	28	LSB ADD 2(hex 3)
	001-11-01-765	19	MSB Gen/Err(hex 4)
	00. -766	22	LSB Gen/Err(hex 6)

B. 11 BOOT CONTROLLER (Cont.)

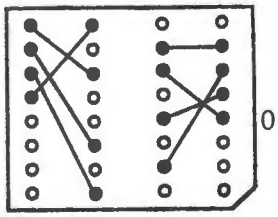
	Part NO.	STB NO.	Function
	001-11-01-767	49	MSB BOOT (hex 1)
	001-11-01-768	31	LSB BOOT (hex 4)
	001-11-01-769	45	MSB EOB (hex 1)
	001-11-01-770	27	LSB EOB (hex 5)

	Part NO.	STB NO.	Function
	001-11-01-771	11	ADD 1 (hex 53)
	001-11-01-772	10	ADD 2 (hex 32)
	001-11-01-773	10	ADD 2 (hex 33)
	001-11-01-774	23	15 Sec. Timer Option

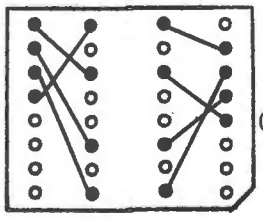
	Part NO.	STB NO.	Function
	001-11-01-778	28	LSB ADD 2 (hex 4)
	001-11-01-779	28	LSB ADD 2 (hex 5)
	001-11-01-780	10	ADD 2 (hex 34)
	001-11-01-781	10	ADD 2 (hex 35)



Part NO.	STB NO.	Function
001-11-02-711	27/28	STB 27 = 1/2 EOB - hex 4 STB 28 = 1/2 ADD 2 - hex 2

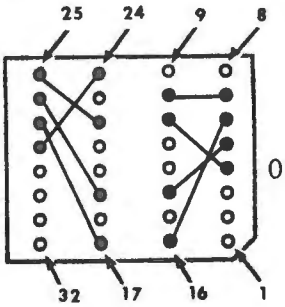


001-11-02-712	27/28	STB 27 = 1/2 EOB - hex 4 STB 28 = 1/2 ADD 2 - hex 3

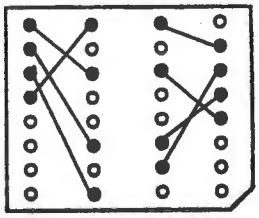


001-11-02-713	27/28	STB 27 = 1/2 EOB - hex 4 STB 28 = 1/2 ADD 2 - hex 4

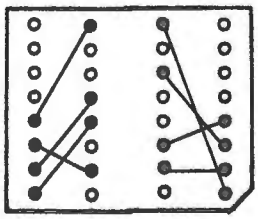
B. 11 BOOT CONTROLLER (Cont.)



Part NO.	STB NO.	Function
001-11-02-714	27/28	STB 27 = 1/2 EOB - hex 4 STB 28 = 1/2 ADD 2 - hex 5

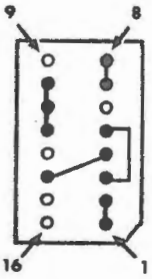
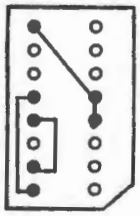
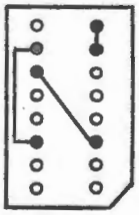
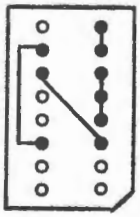


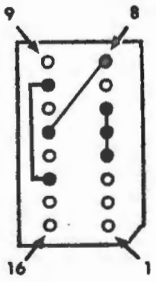
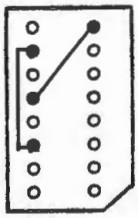
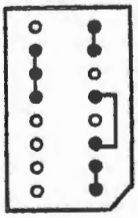
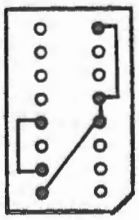
001-11-02-715	27/28	STB 27 = 1/2 EOB - hex 4 STB 28 = 1/2 ADD 2 - hex 6

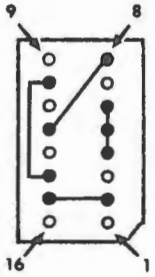


001-11-02-716	45/46	STB 45 = 1/2 EOB - hex 8 STB 46 = 1/2 ADD 2 - hex 6

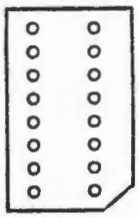
B.12 MULTIPLEXER (DATA FLOW BOARD)

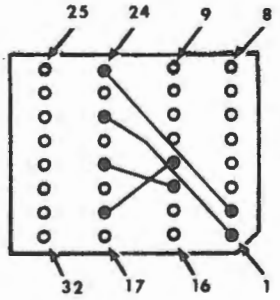
	Part NO.	STB NO.	Function
	001-11-01-723	10	Async Data Sync Data Sets
	001-11-01-724	12	Async Data Sync Data Sets
	001-11-01-725	21	Async Data Sync Data Sets (16 Port MUX)
	001-11-01-742	21	Async Data Sync Data Sets 2400 Baud 8 Port MUX

	Part NO.	STB NO.	Function
	001-11-01-743	21	Async Data - Async Data Sets. 1200 Baud 8 Port MUX.
	001-11-01-744	21	Async Data - Async Data Sets. 1200 Baud 16 Port MUX.
	001-11-01-775	10	Async Data Async Modem
	001-11-01-776	12	Async Data - Async Modem Non Priority Poll Single Xmitt Poll

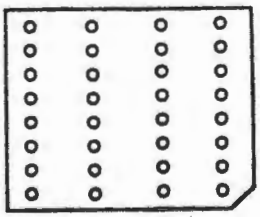


Part NO.	STB NO.	Function
001-11-01-777	21	Async Data - Async Modem - Non Priority Polling - Single Transmitt Poll





001-11-02-709	10	Async Data - Sync Data Sets



APPENDIX C

MISCELLANEOUS CABLE DATA

The cable used between all elements of the INCOTERM SPD 10/20 product line is specified by INCOTERM. Cable types are as shown below; for connector type, cables and wiring see wiring tables attached.

From	To	Type
SPD 10/20	Modem, Multiplexer or Printer	15 Conductor Unshielded Audio Cable, Each Conductor Consists of 7 Strands of 30 Gauge Wire (Belden 8458).
SPD 10/20	Keyboard	25 Conductor Unshielded Audio Cable, Each Conductor Consists of 7 Strands of 30 Gauge Wire (Belden 8459).
SPD 10/20	Program Loader	50 Conductor Unshielded Audio Cable, Each Conductor Consists of 7 Strands of 30 Gauge Wire (INCOTERM CB 1632).
SPD 10/20	Auxiliary Display	6 Conductor (3 pairs) Unshielded INCOTERM Cable, Each Conductor Consists of 7 Strands of 30 Gauge Wire (INCOTERM 1318).

Maximum Diameter of All Types is 1/2 Inch
With an Allowable Bend Radius of 3 Inches.

Each INCOTERM unit connected to an AC source requires a separate grounding buss connector to common system ground.

Table C-1. Typical SPD 10/20 Cable Runs

Unit Type	Typical Cable Length
SPD 10/20	(15 Conductor Cable) 50' - Modem 300' - Multiplexer 1,000' - Multiplexer (OPTIONAL)
KEYBOARD	(25 Conductor Cable) 10' - SPD 10/20
PRINTER	(15 Conductor Cable) 300' - SPD 10/20 1,000' - SPD 10/20 (OPTIONAL)
MULTIPLEXER	(15 Conductor Cable) 50' - Modem 300' - SPD 10/20 1,000' - SPD 10/20 (OPTIONAL)
PROGRAM LOADER	(50 Conductor Cable) 10' - SPD 10/20
AUXILIARY DISPLAY	(6 Conductor 3 Pairs Cable) 10' - SPD 10/20

Table C-2. I/O Cable 15 Wire Conductor, 25 Pin Connector

Belden 8458			E/A RS 232B Standard Interfacing	
Color	Cinch DB 25 P	Cinch DB 25 P	Circuit	Description
Black	1	1	AA	Protective Ground
White	2	2	BA	Transmitted Data
Red	3	3	BB	Received Data
Green	4	4	CA	Request to Send
Orange	5	5	CB	Clear to Send
Blue	6	6	CC	Data Set Ready
White/Black	7	7	AB	Signal Ground
Red/Black	8	8	CF	Data Carrier Detector
	--			
Green/Black	13	13		
Orange/Black	14	14		
Blue/Black	15	15	DB	Transmitter Signal Element Timing
	--	--		
Black/White	17	17	DD	Receiver Signal Element Timing
	--	--		
Red/White	19	19		
Green/White	20	20	CD	Data Terminal Ready
Blue/White	21	21		
	--	--		

Table C-3. Auxiliary Cable 6 Conductor, 25 Pin Connector

INCOTERM 1318

Color	Signal	Cinch DB 25 P	Cinch DB 25 P
Green	H Sync B	15	15
Black	H Sync B Ret.	16	16
White	V Sync B	18	18
Black	V Sync B Ret.	19	19
Red	Sub Video B	21	21
Black	Sub Video B Ret.	22	22

Table C-4. Keyboard Cable 25 Wire Cable 25 Pin Connector

Belden 8459

Color	Signal	Cinch DB 25 P	Cinch DB 25 S	Molex
BLK	KBD D00	1	1	
WHT	KBD D01	2	2	
RED	KBD D02	3	3	
GRN	KBD D03	4	4	
ORN	KBD D04	5	5	
BLU	KBD D05	6	6	
WHT/BLK	KBD D06	7	7	
RED/BLK	KBD D07	8	8	
GRN/BLK	KB ST	9	9	
ORG/BLK	Ground	10	10	
BLU/BLK	KB Present	11	11	
BLK/WHT	+5 VDC	12	12	
RED/WHT		13	13	
GRN/WHT	BELL	14	14	
BLU/WHT	BUZZ	15	15	
BLK/RED	LTD 00			1
WHT/RED	LTD 01			2
ORG/RED	LTD 02			3
BLU/RED	LTD 03			4
RED/GRN	LTD 04			5
ORG/GRN	LTD 05			6
BLK/WHT/RED	LTD 06			7
WHT/BLK/RED	LTD 07			8
RED/BLK/WHT	+5 VDC			9
GRN/BLK/WHT		25	25	

Table C-5. Program Loader Cable 50 Wire 50 Pin Connector

INCOTERM CB 1632

WIRING TABLE

Color	Signal	Cinch DD 50 P	Cinch DD 50 S
BLK	+5 VDC	1	1
BROWN	GND	2	2
RED	OTB 00	3	3
ORANGE	INB 00	4	4
YELLOW	OTB 01	5	5
GREEN	INB 01	6	6
BLUE	OTB 02	7	7
VIOLET	INB 02	8	8
GRAY	OTB 03	9	9
WHITE	INB 03	10	10
PINK	OTB 04	11	11
TAN	INB 04	12	12
WHT-BLK	OTB 05	13	13
WHT-BRN	INB 05	14	14
WHT-RED	OTB 06	15	15
WHT-ORG	INB 06	16	16
WHT-YEL	OTB 07	17	17
WHT-GRN	INB 07	18	18
WHT-BLU	TYP 00	19	19
WHT-VIO	FUNC 00	20	20
WHT-GRY	TYP 01	21	21
RED-BLK	FUNC 01	22	22
RED-YEL	ATTENTION	23	23
RED-GRN	FUNC 02	24	24
WHT-BLK-BLK	RESET	25	25
WHT-BLK-BRN	FUNC 03	26	26
WHT-BLK-RED	ACK	27	27
WHT-BLK-ORG	CONT 07	28	28
WHT-BLK-YEL	BOOT	29	29
WHT-BLK-GRN	INT XX	30	30
WHT-BLK-BLU	INT SEL IN	31	31
WHT-BLK-VIO		32	32
WHT-BLK-GRY	CPT 13 N	33	33
WHT-RED-BLK	CPT 02 N	34	34
WHT-RED-BRN	CPT 18 N	35	35
WHT-RED-RED	CPT 08 N	36	36
WHT-RED-GRN	TURT 4	37	37
WHT-RED-BLU	+14 V	38	38
WHT-RED-VIO	-14 V	39	39
WHT-GRN-BLK	GND	40	40

Table
Table C-5. Program Loader Cable 50 Wire 50 Pin Connector (Cont.)

INCOTERM CB 1632

WIRING TABLE

Color	Signal	Cinch DD 50 P	Cinch DD 50 S
WHT-GRN-BRN	GND	41	41
WHT-GRN-RED		42	42
WHT-GRN-GRN		43	43
WHT-GRN-BLU		44	44
WHT-GRN-VIO		45	45
WHT-BLU-BLK		46	46
WHT-BLU-BRN		47	47
WHT-BLU-RED		48	48
WHT-BLU-GRN		49	49
WHT-BLU-BLU		50	50

NEW DATA

REVISED DATA

BOAC DIFFERENCE DATA

PURPOSE

The purpose of this data is to promulgate information regarding customer changes to the basic manufactured SPD 10/20 Stored Program Display Terminal. The information presented falls into three categories:

1. New data not covered elsewhere in this document.
2. Data which alters the basic description and/or operation.
3. Data which supersedes the basic description.

The method of presenting the three areas of information is:

1. All new data is presented under a heading titled "New Data".
2. Minor differences between the basic description and actual customer hardware are explained under a major paragraph heading identical to that of which the change applies.
3. Data which supersedes a paragraph in total carries a major paragraph heading identical to that of which the change applies.

NEW DATA ITEM 1

KLEINSCHMIDT PRINTER CONTROLLER

General

The Kleinschmidt Printer Controller design provides the Terminal user with the ability to integrate the SPD 10/20 system in an existing or intended environment where the hard copy output is provided by a Kleinschmidt Printer. The controller circuitry is physically located on a standard size I/O circuit board (see Figure 1) and in operation utilizes one I/O controller slot.

Data interface for both transmission of data and reception of control signals is provided by line drivers and receivers which allow the printer to be located up to 200 feet from the Terminal. The line transmitter utilized to interface the character data signals is manufactured by Cermetek, Inc. and is designated the CM 1150. The CM 1150 performs a bipolar line level translation between standard logic levels (0 and +5 volts) to EIA RS 232 B/C levels (+14 and -14 volts). Because the driver is by design a signal inverting device, it is schematically illustrated as an inverter. Figure 2 illustrates the package connections for the dual-in-line CM 1150.

As illustrated, each driver is supplied with two inputs resulting in a nand function; however, when only one input is used, the other can be either left open (high) or tied to the first. There are four CM 1150 circuits utilized in

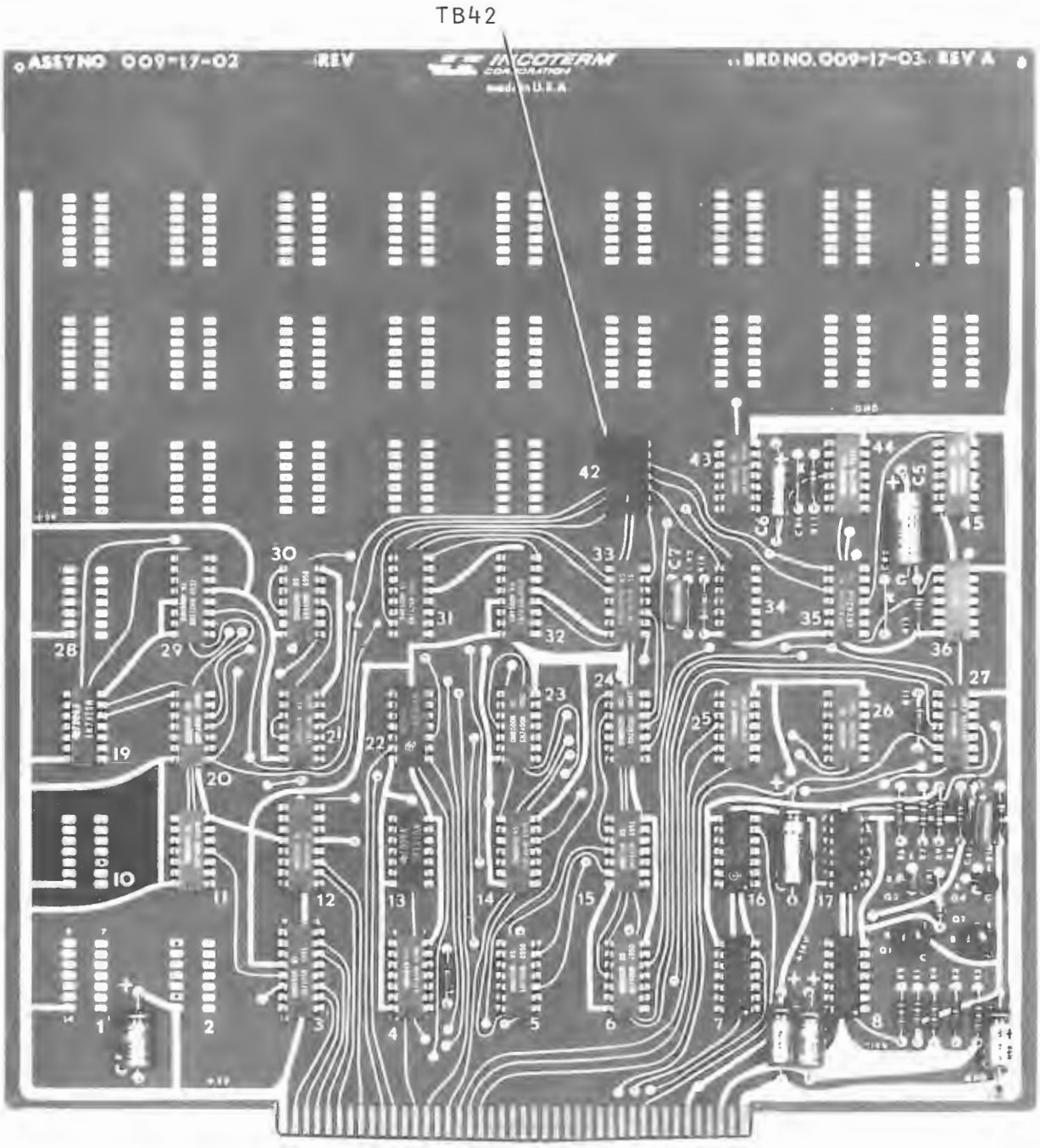


Figure 1. Kleinschmidt Printer Controller

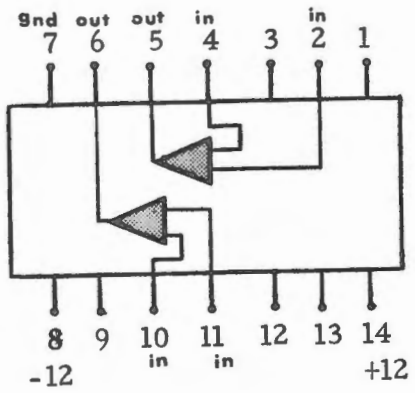


Figure 2. Connection Diagram

the data interface. The TPU data is outputted to the controller on Output Bus bits 00, 01, 02, 03, 04 and 06. The six printer lines are then driven by the line drivers. Control signals which interface between the printer and controller are handled by discrete circuitry which performs similar level translations and provides proper impedance matching (see sheet 3, schematic 009-17-01).

THEORY OF OPERATION

Basic control signal requirements when operating in a Kleinschmidt Printer interface are:

1. The controller must position the printer ribbon.
2. The controller must determine whether the printer is ready to operate.
3. The controller must provide the six bit character data at a stable time.

The following theory of operation references Figure 3, a simplified block diagram, and schematic 009-17-01, sheets 2, 3 and 4.

Referring to Figure 3, it becomes obvious that a minimum circuit complexity is utilized to meet the requirements of Kleinschmidt operation. One factor for this is that the printer itself provides a large portion of the actual operating circuits. As illustrated, the programmed conditions are decoded and the resultant operating mode is fed to the control circuitry. The

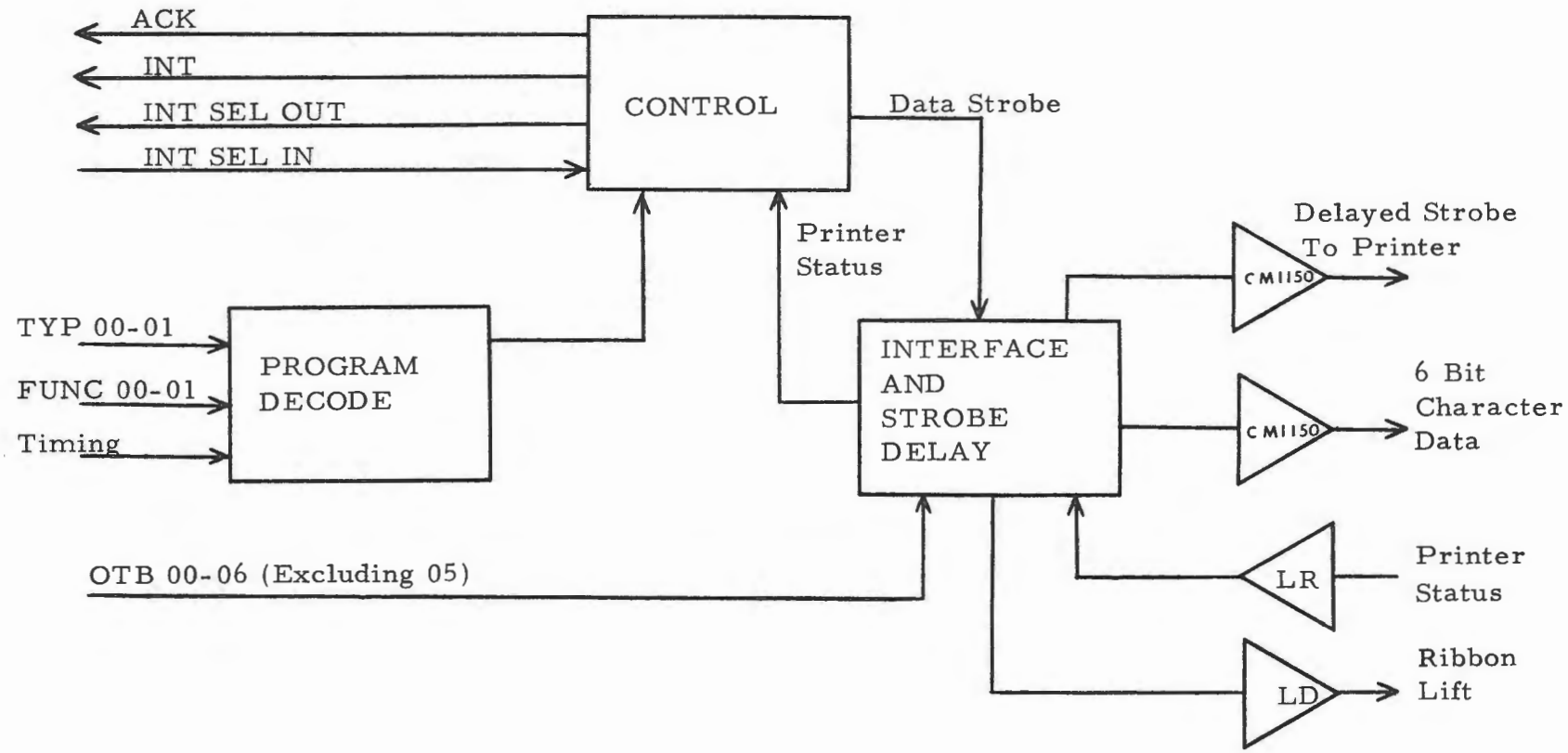


Figure 3. Simplified Block Diagram
Kleinschmidt Printer Controller

control circuitry upon detecting the programmed operating mode, responds with the appropriate signals to the TPU and/or the interface circuit. The interface receives status signals from the printer and forwards the status to the control circuit where enabling or disabling of logic is performed. The interface also includes the character data buffer and associated line drivers and receivers.

Program Decode

Schematic 001-17-01 sheet 2 contains the program decoding circuitry. The TPU programmed, 2 bit TYPE code (00-01) enters the controller circuit board on pins 19 and 21 respectively. The four possible conditions of the TYPE code are decoded at and gates M13 printer Write I/O, M13 printer Test I/O, and M13 printer Control I/O. (The printer cannot input data to the TPU; therefore, a Read I/O is not required.) One enabling leg of each gate is provided by the controller address signal PRADDXX from pin 28 through inverter M4. The logical interpretation of any one of the three gates in a true condition is that the program type decode was addressed to the controller. The true output of the Control I/O decode is inverted at gate M14 and applied to the four gates of M5. Each of the M5 and gates can then be enabled by a particular programmed four bit FUNCTION code (00-03). Similarly, the T I/O, when true, is inverted and fed to M23 as an enabling signal. The other leg of M23 is the result of oring various tested conditions which produce a T I/O Acknowledge (ACK). The four bit FUNC code enters the controller at pins 20, 22, 24 and 26, bits 00-03 respectively. Table 1 lists the TYP and FUNC code bits with appropriate decoded command.

There are two ways in which to achieve a controller reset condition. One is by receipt of a TPU reset command at pin 25. The general I/O reset is inverted at M4 and applied to pin 2 of and gate M6. Pin 1 is enabled on a timing phase 18 clock signal. The true condition of M6 is inverted at M4 and enabled through or gate M24 from which it is distributed as the printer reset signal. The other method is by programmed reset. And gate M24 (PRCIR) is enabled by detecting a C I/O 5, which is ored through M24 and distributed as

Table 1. TPU Programmed Control Codes

Type Code		Function Code				Description
Binary	Weight	Binary	Weight			
2	1 (LSB)	8	4	2	1(LSB)	
1	1					W I/O
1	0					(normally R I/O Not Used
0	1	0	0	0	1	C I/O 1 = Disable
0	1	0	0	1	0	C I/O 2 = Initiate Print
0	1	0	1	0	0	C I/O 4 = Mask Interrupt
0	1	0	1	0	1	C I/O 5 = Reset
0	1	1	0	0	0	C I/O 8 = Unmask Interrupt
0	0	0	0	0	0	T I/O = ACK
0	0	0	0	0	1	T I/O 1 = Ready
0	0	0	0	1	0	T I/O 2 = Not Ready
0	0	0	1	0	0	T I/O 4 = Paper Low

in the prior case. One of the reset lines is applied to latch M15/M23 PRDSAB/ PRENAB (printer disable, enable) and latch M15/M23 PRMSK/PRUMSK (printer mask, unmask). These two latches are set by decoded program codes. The reset signal is routed to sheet 4 where strobe and delay circuitry are reset and sheet 3 where the ready data flip flops and interrupt circuitry are reset.

Timing phase 2 enters the controller at pin 34 and is fed to and gate M20 where it enables the inverted W I/O Ready signal from gate M21 and resets an interrupt at the end of a W I/O. TURT 4 enters the controller at pin 37 and is fed to sheet 3 as the READY 1-2 flip flop clock.

Control Circuitry

Schematic sheet 3 illustrates the control logic portion of the controller. The INT SEL IN signal enters the controller at pin 31. The first time the SEL IN is true (low) the condition is inverted at M14 pin 4 from which the now high signal is fed on one path to the INT SEL OUT gate M21, ALLOW INT gate M30, and the clock input PRINTER INTERRUPT SELECT HOLD on flip flop M29. The other path is through another inverter M14, at which the signal on pin 12

is identical to the true signal on input connector pin 31. The double inverted signal is fed to the clear input of the Back to Background flip flop M31. The clock provided for M31 is originated at the output of gate M23, Printer Acknowledge. The $\overline{Q}$ side of M31 is high after the TPU enters background and selects have been issued, thereby clearing the background flip flop. When the Printer is ready, operation will continue. But the conditions for enabling gate M33 (Ready) have not yet occured and latch M33 is still in an initial Reset state. Until further conditions occur, the TPU operates in the background mode.

When the TPU issues a Write I/O addressed to the printer, the true condition of gate M13 (PRWIO) is fed directly to the Ribbon Lift circuitry on sheet 4 which complies with the requirement that the ribbon be lifted prior to data transfer; therefore, that condition must be true (ribbon lifted) to enable the Ready circuitry on sheet 3. The printer status, Ready latch condition (not ready) and ribbon lift signal is anded at gate M35 which enables the 40 ms delay and ultimately M35 pin 8 becomes true. The fact that M33 pin 6 is low (not ready) is anded with the Ready signal (low true) at gate M24. The input conditioning of Ready flip flop 1 is J = 1, K = 0. Ready flop 2 had previsouly been cleared to $\overline{Q}$ high so on the next T4 clock pulse gate M33 PRRDC sets the latch to the Ready state and the next INT SEL IN will enable the ready circuit.

The high output of PRRDA sets the J side of the interrupt select hold flip flop resulting in the Q side high anded with the unmask signal at gate PRASH. The PRASH, when true, is low so the INT SEL OUT is not enabled, but the low is inverted at PRASH I where anding occurs with the INT SEL IN (high) and Printer Interrupt B bow tie gate sets low, resulting in an interrupt at pin 30. The Ready signal (high) is also anded with the W I/O at gate PRWIRD, a W I/O. Ready ACK is sent from pin 27 and signals PRWIRD and PRWIRD I are sent to sheet 4 as the data register output strobe.

Signal Interface

Signal PRWIRD (Printer (W I/O Ready) is provided to the data buffer register PRSB0-PRSB5 as the register clock. In addition to strobing the

register, the signal is anded with timing phase 13 at gate M26. The output signal of M26 initiates a one shot time delay. The duration of the delay is determined by the time constants of R14 and C7 and is calibrated at 150 microseconds. M20 decodes the delay condition and enables the strobe to the printer through line driver M16. The resulting delay has thus insured that the character data at the printer is stable before printing is performed.

As soon as the printer starts printing, a busy signal is sent to the controller and enters the circuit on pin 58. In addition to being part of a T I/O circuit, the busy signal is sent to M29 to reset the strobe circuit. Another condition available to reset M29 is on Power Up which is detected at M45. The delays of M44 and M36 are designed with a provision that allows regeneration of the ribbon lift signal if another W I/O is detected, thereby keeping the ribbon in the operating position when continuous operation is desired.

Input pins 60 and 62 detect a contact closure which is signaled from the printer when a low paper condition exists. If the printer is unavailable, gate M26 provides the proper output which is program detected by a T I/O 2.

Kleinschmidt Controller Test Points

TP	
1	H = Initiate Print (C I/O 2) L = Disable (C I/O 1)
2	H = Unmask (C I/O 8) L = Mask (C I/O 4)
3	H = READY L = RESET
4	H = TPU in Background
5	H = Data Flops True Ready Will Be Set
6	L = $\overline{\text{Set Ready Flops}}$
7	H = Strobe Data W I/O Ready L = Strobe Data Buffer
8	H = 150 microsecond delay
9	H = 40 millisecond delay
10	H = 500 millisecond delay

NEW DATA ITEM 2

CYCLIC CHECK CONTROLLER

GENERAL

The Cyclic Check Controller provides a means of verifying whether a transmitted data message has been correctly received. The communications transmitting system develops the check character by serially feeding each character into a logic polynomial equiation. The final result is transmitted after the last data character in the message. The receiving end performs an identical operation on each inputted data character until the final check character has been entered. The receiving electronics then compares its computed cyclic check character with the transmitted cyclic check character and, if identical, the data is accepted.

The Cyclic Check Controller is located in the I/O controller section of the TPU and physically conforms to the standard I/O circuit board size (see Figure 1). Since the controller resides in an I/O position but is interrupt controlled by a communications controller, pin 31 is jumpered to pin 32, providing passage of the Interrupt Select signal. With reference to Figure 2, the Cyclic Check Controller Block Diagram, the following table lists the controller interface signals.

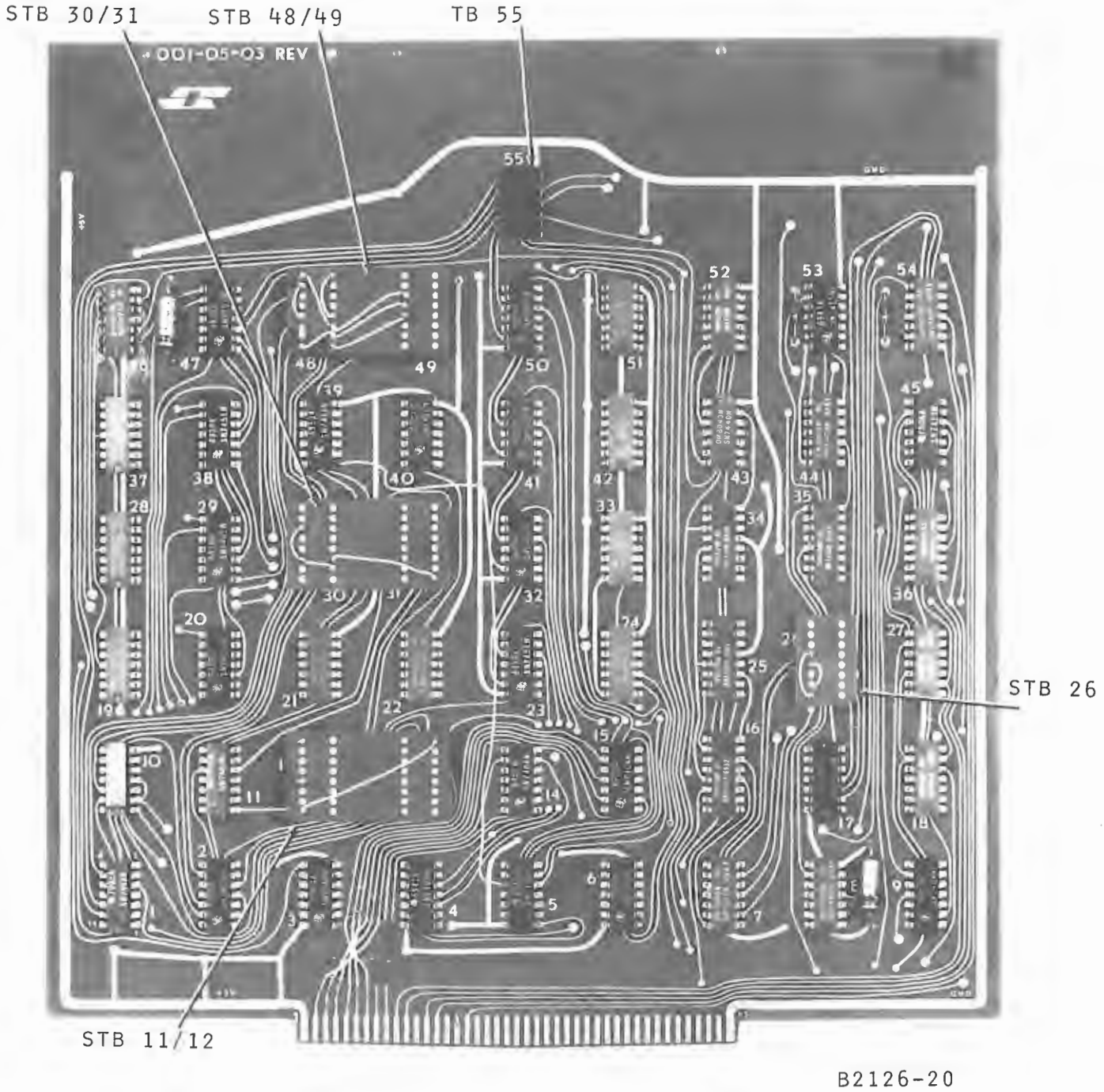


Figure 1. Cyclic Check Controller

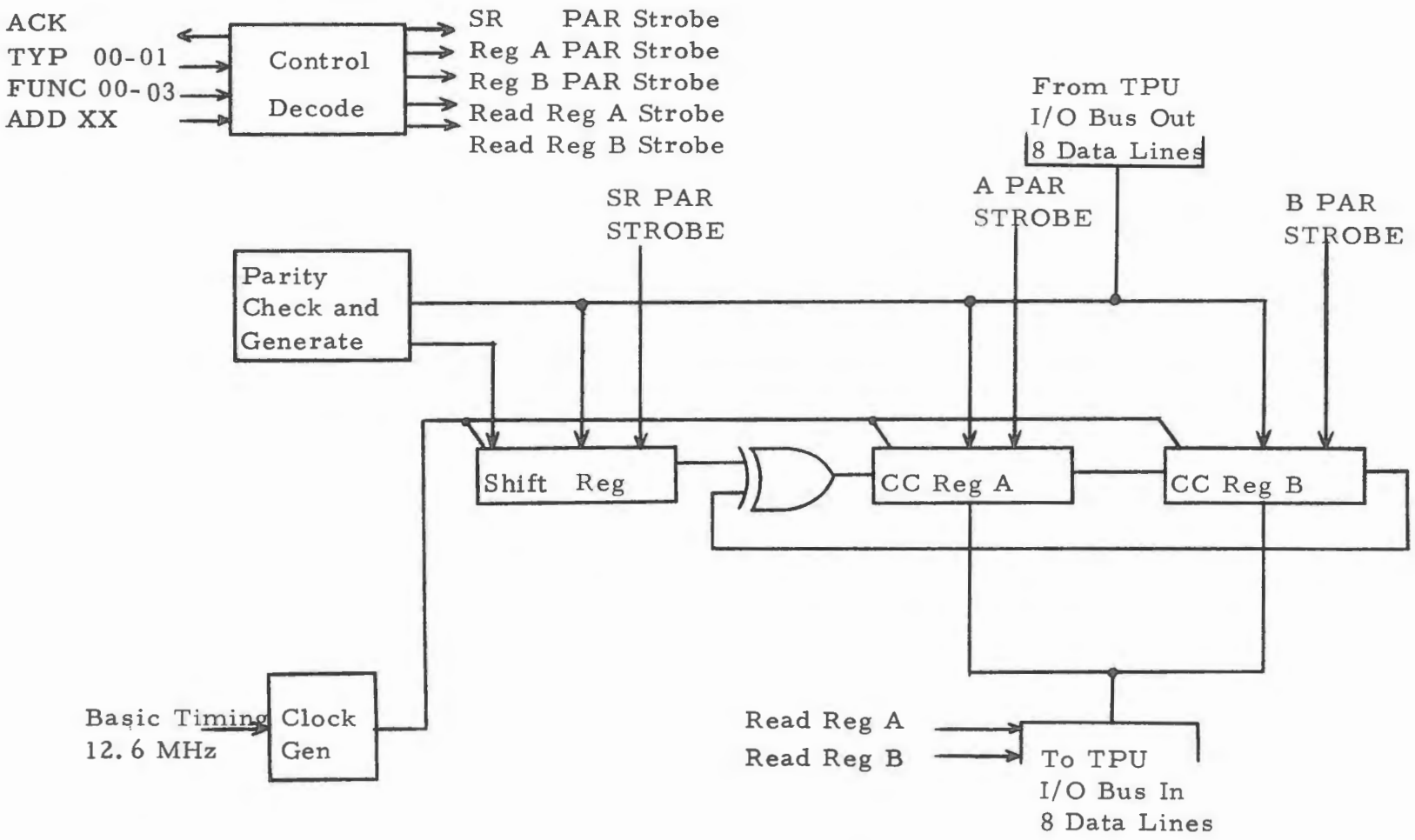


Figure 2. Block Diagram, Cyclic Check Controller

Table 1. Cyclic Check Controller Signals

Signal	Lines	Routing
Bus In	8	To processor
Bus Out	8	From processor
Function	4	From processor
Type	2	From processor
ADDXX	1	From processor
Clock	4	From processor
ACK	1	To processor
Ground	1	From processor
+ 5 VDC	1	From processor

Referring to Figure 2, the following are the basic components and a brief description of operation:

Control Decoder- The decoder receives programmed commands which specify the mode of operation. The two TYPE bits, four FUNCTION bits and address strobe are converted to the various commands illustrated.

Internal Clock Generator- The internal clock is a timing derivative of the basic system timing and can be optioned for six, seven or eight bit data. The selected clock rate serially shifts data from the SR into the cyclic check registers.

Parity Circuit- The parity circuit generates parity for the cyclic controller when data is to be outputted and checks the parity of data received by the Terminal.

Cyclic Check Register- The cyclic check register is a 16-bit register (bit length optional) with optional exclusive OR circuits. The register can receive parallel data directly from the TPU Bus out lines or serial data from the shift register (the serial path is the cyclic check path). The register presents data on the TPU Bus in lines.

Shift Register- The SR is a parallel in, serial out, shift register. The input is the TPU Bus in data which is serially shifted into the cyclic check register.

THEORY OF OPERATION (Reference Schematic 001-05-01)

The electronic circuitry schematically illustrated on sheet 2 performs the controller program decoding. The TYPE code, being a two bit code, offers a possibility of four decodes:

W I/O	(Write)
R I/O	(Read)
T I/O	(Test)
C I/O	(Control)

The TYPE decode is ANDed with one of the 16 possible FUNCTION decodes to provide the programmed operating mode. TYPE bit 0 and bit 1 enter the controller on pins 19 and 21, respectively. The two bits are single and double inverted at M36. Single inverted inputs are fed to M45 pins 1, 11 and 13. Double inversions are applied to pins 3, 5 and 10. The remaining leg of each AND gate is enabled by the signal ADDXX which, when true, logically indicates that the command is pertinent to the cyclic controller. The addressing signal is input to the circuit board on pin 28 and is inverted at M38 (pins 8 and 9).

The W I/O decoded output from pin 12, M45 is fed to AND gates M52 (2), M18 (2) and M27. With the exception of gate M27, the enabling leg is the programmed function code. M27 is enabled on a phase 13 clock pulse. The first bit of the FUNC code (00) enables leg 8, M52 and results in the logical ANDing of a W I/O and FUNC 1. The decoded command at pin 10 will enable the data on the Bus Out lines from the TPU and store it in the most significant byte of the cyclic check register (register A). The strobe generated at pin 10 is CCRA PAR Enable. The signal CCRA PAR Enable also conditions pin 1, M8 and on a T9 clock (pin 2) pin 3 is enabled through OR gate M3, pin 12 and strobe CCRA is enabled. The data at the D input, as a result of CCRA PAR Enable, are thus strobed into the register on T9 by the CCRA strobe. The data word entered can be from six to eight bits in length.

The W I/O decode at gate M52 output pin 13 is a W I/O function 2. The signal enabled is CCRB PAR Enable and performs the same function as that previously followed for the cycle check register A. In this case, however, the B register (least significant byte) is operated upon.

The decode at M18 pins 2 and 3 is a W I/O and FUNC bit 02 (W I/O4). The pin 1 output enables OR gate M27. After passing through inverter M7, the resulting signal (W I/O ADDXX [F2 + F3]) is applied to pin 9, M8; pin 5, M7 and fed to the J input M35, sheet 4. On the next T9, M8 is conditioned, which enables pin 13, OR gate M6. The strobe generated (SR STROBE) enables TPU data into the shift register M4, M5. The seven LSB's are considered for parity, odd or even, and the resulting parity bit is detected at M17, enabled through AND gate M54 (pin 6) and OR gate M54, pin 8, from where it is fed to shift register M4 as the seventh bit. Parity is not generated for six or seven bit words.

The highest order function bit (03) is ANDed with the W I/O at AND gate 18, pins 5 and 6. The decode W I/O 8, when true, produces at pin 4 a signal which is routed through OR gate M27, producing a strobe, as in the W I/O 4 decode. The decoded signal is also fed to pin 1, M54 and inverter M53, pin 3. If parity is incorrect, status flip flop M35 is set. It is unnecessary to check parity for six or seven bit words.

The status flip flop is reset by a System reset signal applied at OR gate M54, pin 13 or at timing phase 2 ANDed at gate M44 with FUNC 01 and an addressed T I/O which is detected at AND gate M27.

The System Acknowledge signal is a function of Or'ed conditions at gate M43. All W I/O commands are acknowledged (pin 10). All R I/O (Read) commands are acknowledged (pin 9). T I/O 1 (decoded at M44) is acknowledged only if the controller is present (M43 pin 12). T I/O 2 (decoded at AND gate M27 pin 13) is acknowledged through AND gate M44 pin 11 if no error is detected at status flip flop M35 (M43 pin 13).

The TYPE programmed Read I/O signal is decoded and ANDed with the address line at gate M45, pins 9, 10 and 11. The output of the decoded R I/O is fed to sheet 3 AND gates M18. At M18 the R I/O is ANDed with

FUNC bits $\overline{00}$ and $\overline{01}$ resulting in two Read commands, R I/O 1 and R I/O 2. R I/O 1 enables data from the MSB (register A) to the TPU input Bus and R I/O 2 enables data from the LSB (register B) to the input Bus.

The T I/O decode occurs at gate M45 pins 3, 4 and 5. ANDing with the programmed FUNC bits 00 and 01 result in two tests, T I/O 1 (controller present) and T I/O 2 (error status).

FUNCTIONAL OPERATION (6 bit data)

When operating in a communications environment with 6-bit data, there is no parity, therefore the generation and checking circuit is not used. Initializing the controller circuitry is accomplished by programming a W I/O 3 with all data bits equal to zero. The W I/O 3 is effectively a W I/O 1 and 2 derived at gates M8 where the strobes for A and B registers are enabled. The first character to be cyclic checked is parallel enabled to the serial register by the programmed W I/O 4. After the data has been entered in parallel, a serial shift-right is initiated which enters the data into CC Reg A. When the shift is complete, parallel entry and subsequent shift occurs until the entire data train is complete. If the SPD 10/20 is to transmit the data, a Read I/O is issued, enabling the cyclic check character to the input Bus. The other case is when the data is being received, at which time the last character received is the cyclic check character. The check character is strobed from the CC REG by the R I/O command and if the data has been received without digital distortion, ie. dropped bits, the character is all zeros.

NOTE

> Depending on whether a six or twelve bit check is performed, both registers A and B may be used.

OPERATION WITH 8 BIT DATA

Initialization is accomplished by loading all zeros in the CC REG, as in the previous case. The seven LSB's of the first character in the data train are parallel entered into the SR. The parity bit (odd or even, depending on the option) is placed in the MSB. The character is then serially shifted

into the CC REG. As remaining characters are entered, the data is circulated and comparisons are made at exclusive OR gates. The results of the re-circulating data comparison are cumulative and the last data residing in the CC REG is transmitted as the cyclic check character.

In the receive mode, after initial clearing, the first character is entered in the SR by a W I/O 8 command. All eight bits are parallel enabled to the SR. At the same time, the input data is also available to the parity circuit. If an error is detected, the parity status flip flop is set. After the first character is entered, the bits are serially shifted into the CC REG, at which time the controller is programmed to test the parity status with a T I/O 2 command. This process is repeated for each character in the data train. The last character entered is the cyclic check character (in the case of a 16-bit check, the last two characters are check characters). If the data message is without error, the cyclic check comparison is all zeros.

MULTIPLE CYCLIC CHECK MODE

If more than one check is to be performed, a core memory location is required to store the contents (cyclic check character) of the CC REG. The core requirement increases to two locations for 12, 14 or 16 bit data. Assuming the data to be transmitted is eight bits, the cyclic check polynomial is 8 bits and two checks are desired; both CCA and CCB are used. One core location is reserved for CCA (SA) and another for CCB (SB). Both locations SA and SB are initially loaded with all zeros. SA is enabled to CC Reg A. The first character is then loaded into the shift register. The results of Reg A are then returned to core location SA. The same process is performed on Register B and its associated core location. The process is continued for all character data A and B. After all characters have been cycled, the check character for A and B is located in their respective core locations.

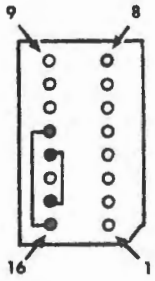
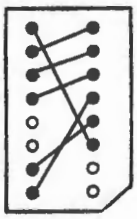
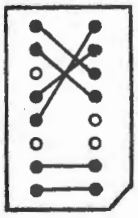
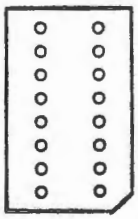
CYCLIC CHECK CONTROLLER TEST POINTS

The test points are located at block position 55 on the cyclic check controller printed circuit board.

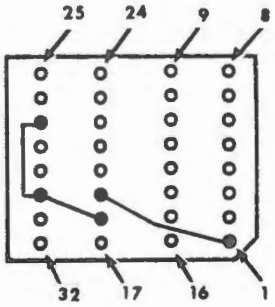
Table 1. Test Point Identification

PIN	Signal	Signal Level
1	Service Strobe	L = CC REG Entry Enable
2	CCRB Strobe	H = Clock Register B
3	SR PAR Enable	H = Serial/Parallel Register Mode Control
4	M35 Q Side	H = Timing Reset
5	Parity Bit	H or L depending on odd or even option
6	SR Strobe	H = Shift Register Strobe
7		
8	$\overline{\text{R I/O} \cdot \text{ADDXX} \cdot \text{F01}}$	H = Strobe In B Register Data
9	$\overline{\text{R I/O} \cdot \text{ADDXX} \cdot \text{F00}}$	H = Strobe In A Register Data
10	status	L = Good Data ACK
11	CCRA Strobe	H = Clock Register A
12	CCRA PAR Enable	H = Enable A Input Data
13	Serial Shift Enable	H = Shift Data In Register
14	CCRB PAR Enable	H = Clock Register B

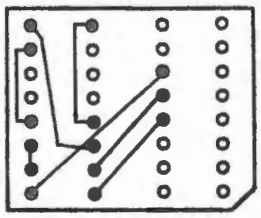
CYCLIC CHECK CONTROLLER OPTION BLOCKS

	Part NO.	STB NO.	Function
	001-11-02-703	26	6 Bit Word Length No Parity
	001-11-01-801	57	6 Bit Word Length MSB to LSB Check
	001-11-01-802	56	6 Bit Word Length MSB to LSB Check
			

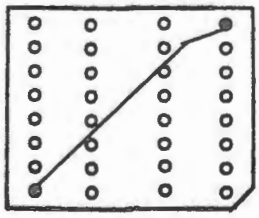
CYCLIC CHECK CONTROLLER OPTION BLOCKS



Part NO.	STB NO.	Function
001-11-02-763	30/31	6 Bit Word Length 6 Bit Polynomial (x^6+x^5+1)



001-11-02-764	48/49	6 Bit Word Length 6 Bit Polynomial (x^6+x^5+1)



001-11-02-765	12/13	6 Bit Word Length 6 Bit Polynomial (x^6+x^5+1)

NEW DATA ITEM 3

DUMMY CONTROLLER

The Dummy Controller (sometimes referred to as a jumper board) is a printed circuit board which conforms to the standard I/O controller physical size. Figure 1 illustrates the Dummy Controller number 001-10-24. Use of this controller enables the programmer to include all I/O slot locations in his program. For slot locations in which an active controller is not contemplated, the dummy is inserted. The result is that when the TPU selects a controller further down the addressing chain than an unused I/O slot, the INT SEL IN signal is sent which the dummy routes to the INT SEL OUT line as an active controller would if service is not desired. This effect is accomplished by wiring on the curcuit board which jumpers connector pins 31 and 32.

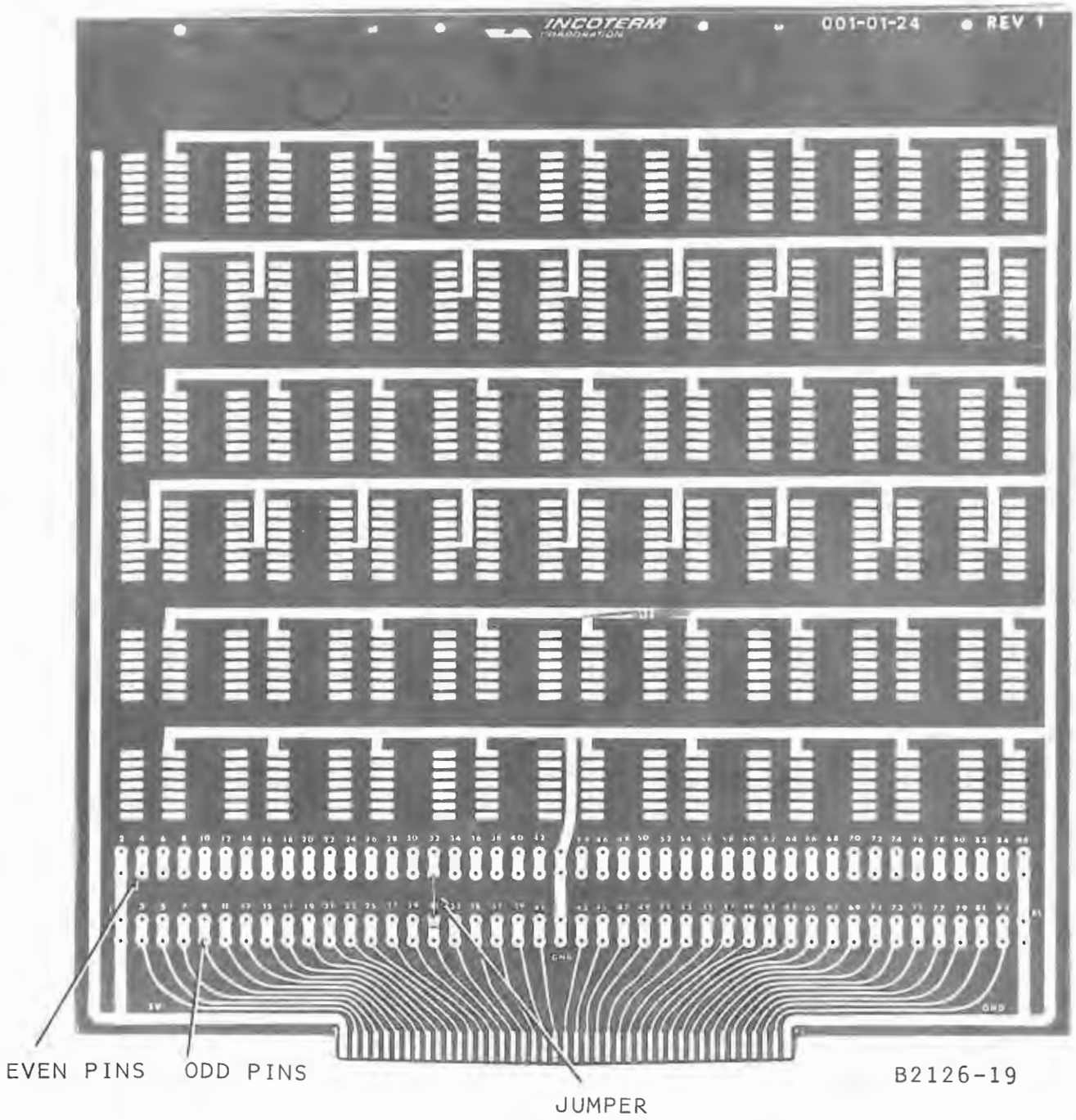


Figure 1. Dummy Controller

NEW DATA ITEM 4

POWER INDICATION

Fuse

The BOAC configured SPD 10/20 Stored Program Display Terminal contains a main ac line fuse which provides a visible indication upon failure. This fuse is located on the input/output connector panel between the last I/O connector location (#10) and the male ac input receptacle (for location see Figure 2-6, page 2-7). The indication is accomplished by mechanical means rather than electrical. Actuation occurs when an overload current is passed through the fuse link. The fuse link is spring loaded and when an overload occurs (blown fuse), the spring releases a small rod which travels into the plastic viewing port, which provides a positive indication of the fuse condition. See Figure 1 for a view of the mechanical indicator fuse and holder assembly.

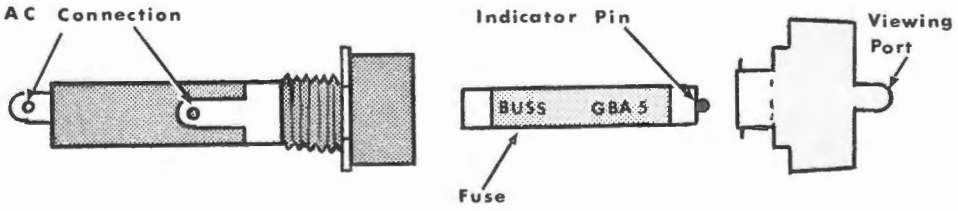


Figure 1. Indicating Fuse, Install Pin Toward Viewing Port

PILOT LAMP

The pilot lamp assembly is an optional device designed to indicate the presence of ac power ON and is available on both main and auxiliary Displays. As illustrated in Figure 1, the lamp is a neon glow tube and is connected across the 115 volt output distribution point of the power supply. Input can be from 115 to 230 volts ac. In keeping with the aesthetic value of the Terminal, the lamp is physically located behind the bezel screen in the right side of the Terminal, above the ON-OFF switch. The lamp assembly is a molded unit; therefore, should replacement of a faulty lamp be desired, the unit is completely replaced.

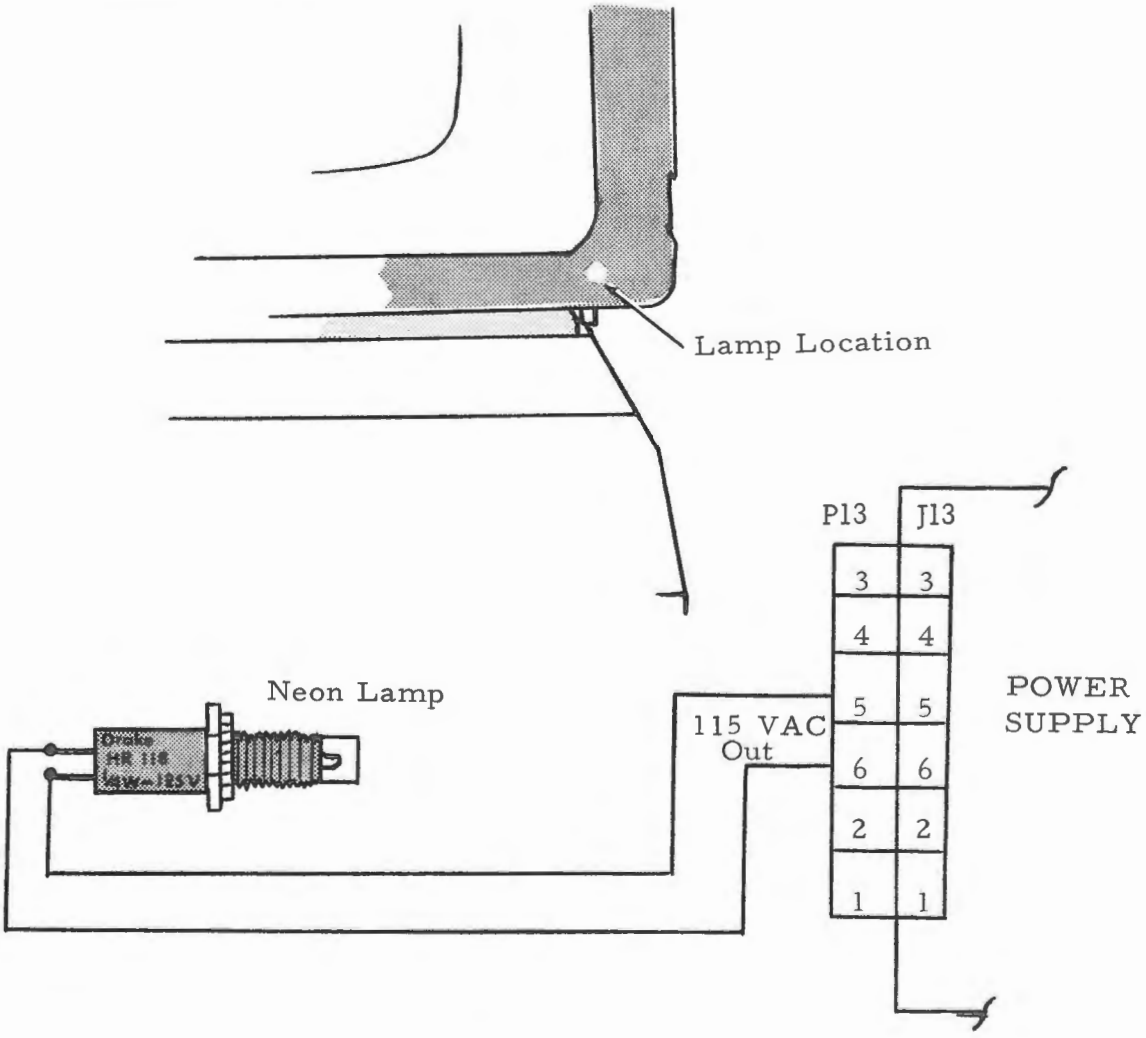


Figure 1. Optional Neon Lamp Power Indicator with Power Supply Connections

NEW DATA ITEM 6

AUXILIARY POWER SUPPLY

General

The Auxiliary Power Supply provides operating voltages to the monitor exclusive of the monitor circuitry. This supply is utilized in a 50- 60 Hz environment and eliminates flickering which may otherwise occur. The technology applied to this supply is similar to the main Terminal power supply (see paragraph 5.6, this section). However, since not as many operating voltages are required, far less components are used. The commonality of the main and auxiliary chassis allow installation of the supply in the same location as that designed for the main Terminal supply.

Theory of Operation

Input ac is connected to the Auxiliary Display at connector J13, which is commonly of the twist lock variety. Dedicated pin connections on J13 are polarized as follows:

PIN 1 Connects to the common or neutral ac wire
PIN 2 Connects to the high side of the line (Hot)
PIN 3 Connects to power ground

The input transformer T1 (reference schematic 012-13-01) has split primaries (two) which are tapped for various input potentials. By connection of jumper leads, the phased potentials provide a range of input voltage as illustrated in Table 1.

Table 1. T1 Input Interconnections

Nominal AC Line Voltage	Transformer T1 Jumper Connection	AC Input (J13-2 Conn.)
105 VRMS	4-8, 3-7	T1-7
110, 115 VRMS	4-8, 2-6	T1-6
120, 125 VRMS	4-8, 1-5	T1-5
210 VRMS	4-7	T1-3
220, 230 VRMS	4-6	T1-2
240, 250 VRMS	4-5	T1-1

T1 provides three secondary ac voltages, two of which are rectified and provide dc operating voltages with the third providing the 6.3V ac Filiment voltage for the cathode ray tube.

Fullwave rectifier CR1 produces a positive dc voltage at power supply jack 3 pin 1 (see Figure 1) with capacitive filtering at C1. Regulator M1 is a Fairchild MA723C, which produces a regulated +24 volt output. Overcurrent conditions are sensed by the voltage drop across R6, a 0.25Ω resistor which feeds a voltage level to the current sense input of M1 (pin 2). Upon sensing the overcurrent condition, M1 causes the bias change necessary to open circuit Q1. Overvoltage conditions are detected by VR1, a 27 volt zener diode. When the +24 volt line rises to the +27 volt level, the diode conducts and a current is caused to flow through R10. The resulting voltage drop (E = IxR) across R10 enables the gate of S1 (a silicone controlled rectifier). The potential causes CR2 conduction and M1 internally opens Q1. When the SCR has been fired, the only way to normalize the condition is to disrupt the anode supply potential through R1. This can be accomplished by turning the unit OFF momentarily. Capacitor C3 decouples the power supply +24 volt line at the output pin J2-5. The output voltage can be adjusted at R8, a 2K potentiometer.

Full wave rectifier CR4 provides the positive voltage for the +73 volt circuit. Component M3, a Fairchild circuit, performs the regulation and circuit protection. Overcurrent conditions cause a voltage drop across the

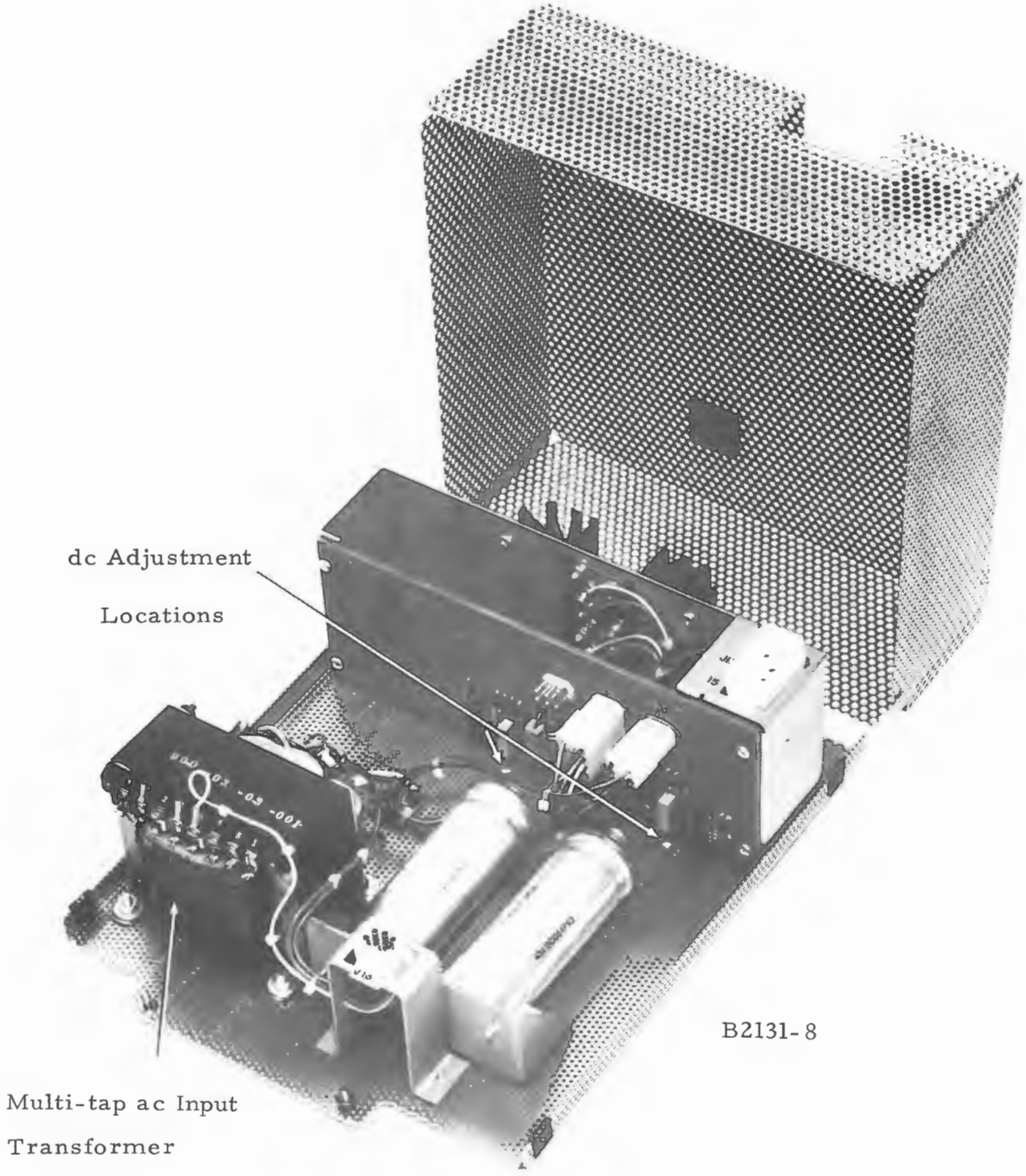


Figure 1. Auxiliary Power Supply

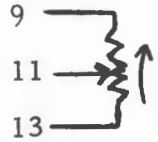
.44Ω resistor R17. The resulting voltage is sensed at M1 pin 3 and Q3 is open circuited. Overvoltage protection is provided by VR4, an 80V zener diode. If the output level should rise to the zener value, conduction occurs and a voltage drop is present across R23. The voltage is fed to the gate input of S3, an SCR. The SCR, when fired, enables the voltage divider R12 and R13 which biases the circuit for subsequent shut down. As in the case of the +24 volt operation, circuit reset is accomplished by momentarily powering OFF the input a. c. Additional protection is provided by VR3 at the base of Q4, which limits that point to 36 volts when the output voltage is shorted. The output voltage level can be adjusted at R22, a 10KΩ potentiometer and output decoupling is provided by C7 at J2 pin 8.

NEW DATA ITEM 7

WIRING DIAGRAMS

MONITOR CONNECTOR WIRING

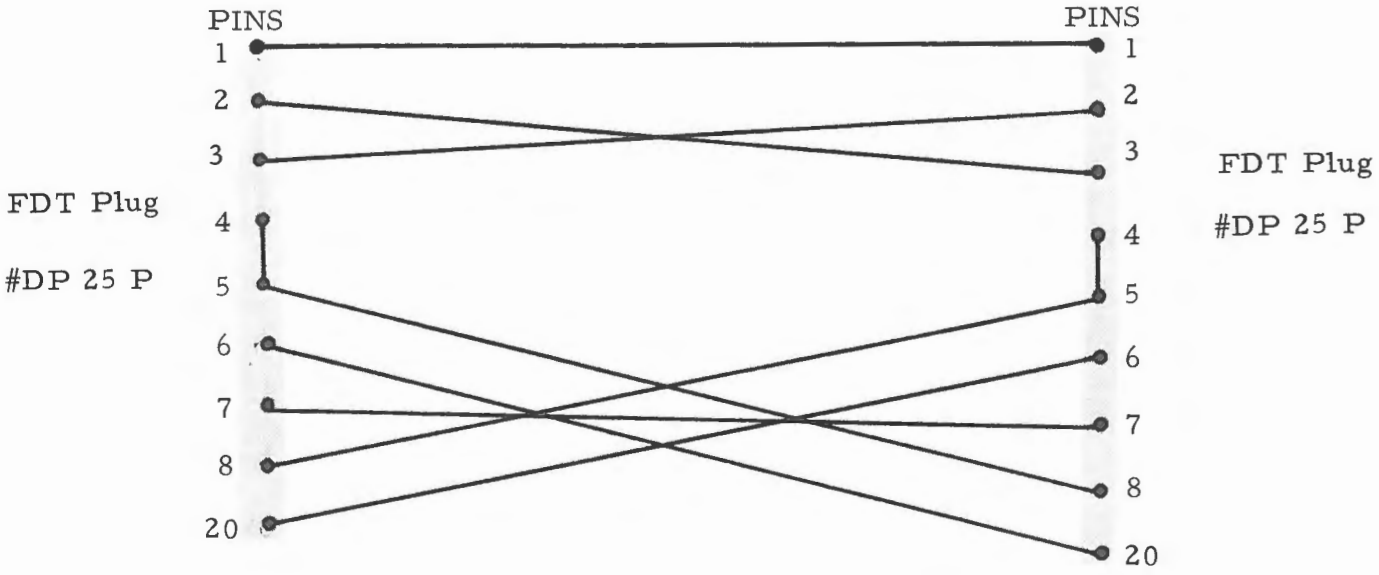
Pin	Signal
7	6.3 VAC
8	6.3 VAC return
9	To potentiometer 9
11	11
13	13
15	Horizontal Sync
16	Return
18	Vertical Sync
19	Return
21	Video
22	Return
23	+73 V
24	+24 V
25	Return to ground for +73 and +24 Volts



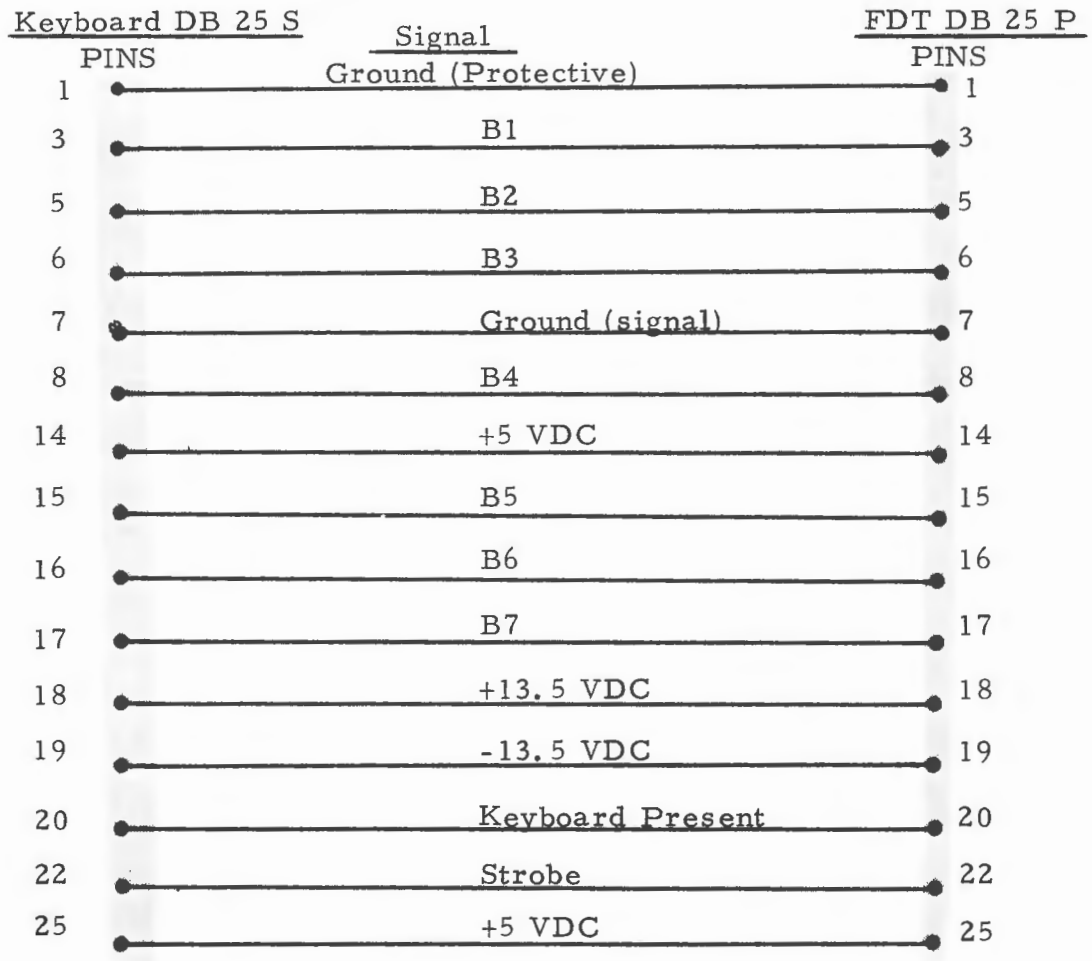
Clockwise position is highest brightness

Auxiliary Cable, drawing 004-10-09, same as Technical Manual Table C-3.

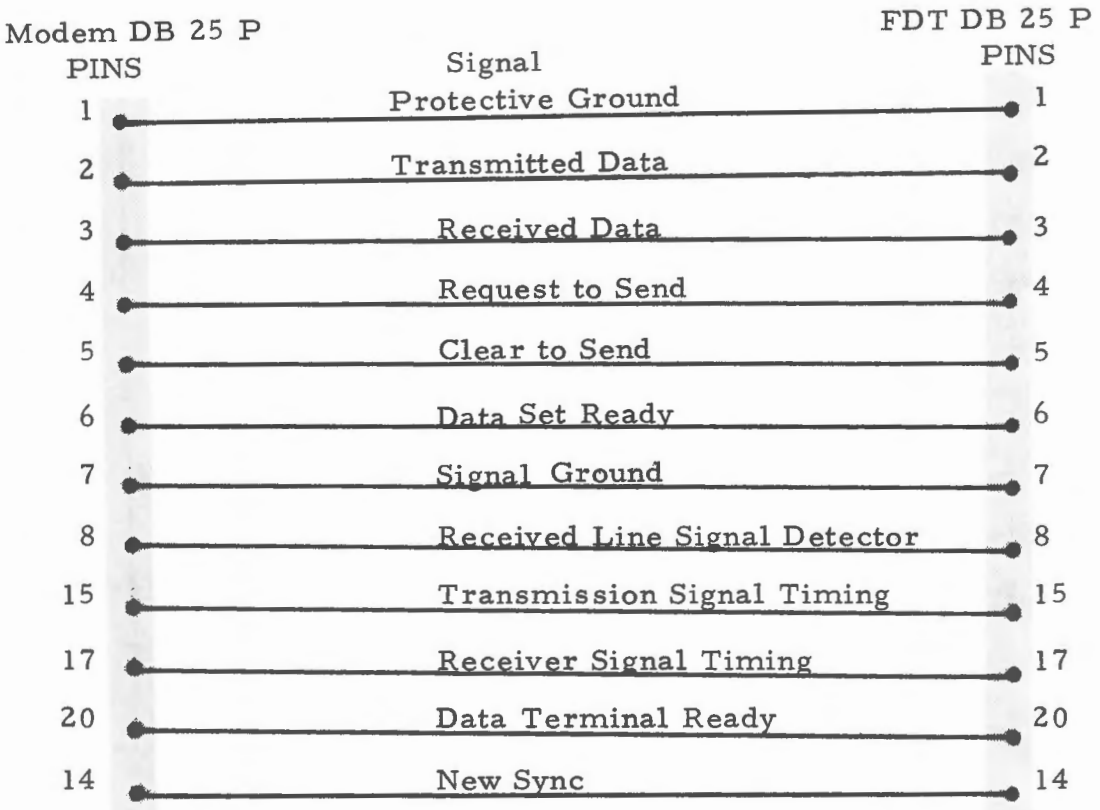
Half duplex operation directly connecting two free standing displays. Reference cable drawing 001-10-92. This cable for asynchronous operation only.



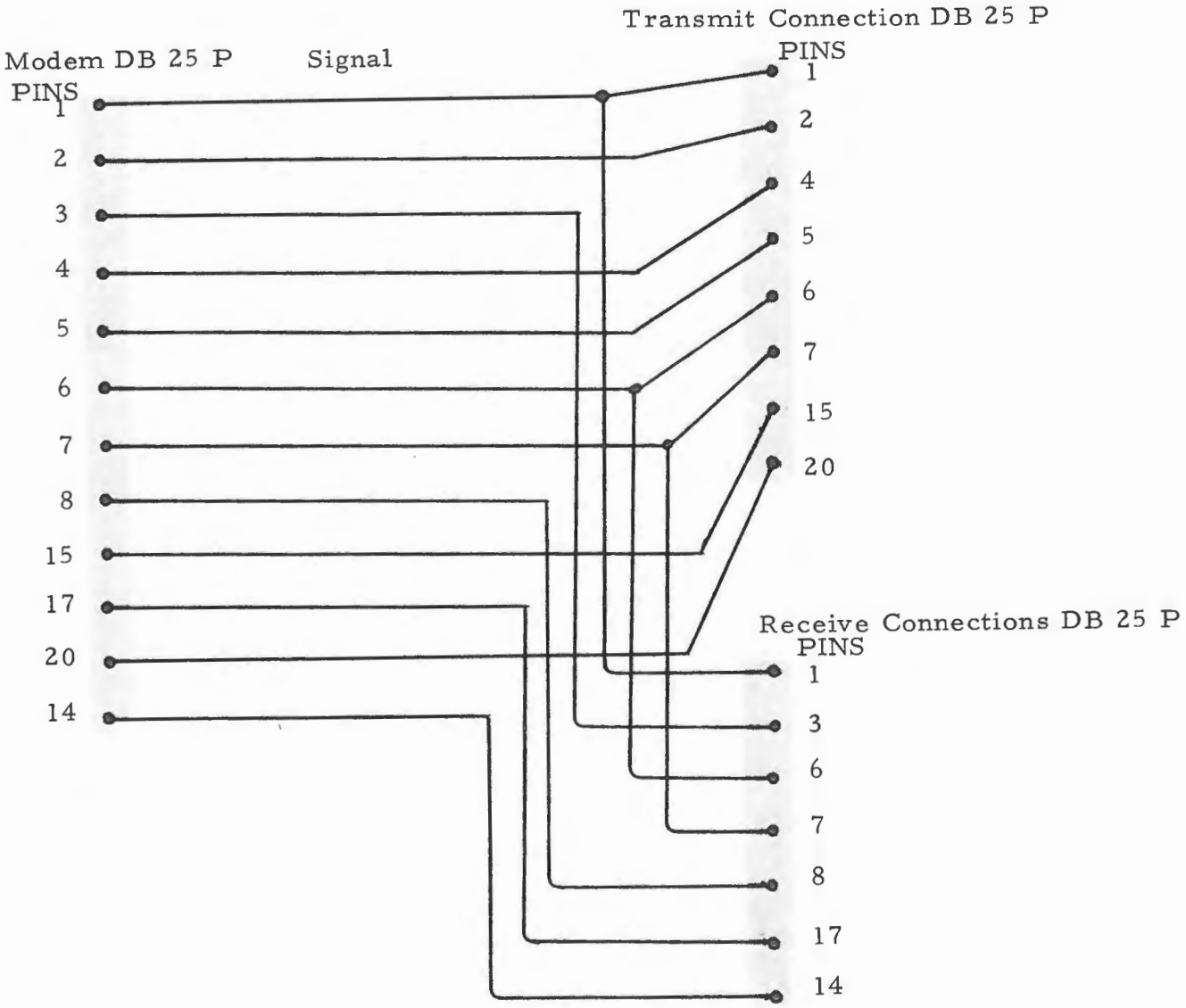
Freestanding Display Terminal cabling diagram. Reference drawing number 011-10-07.



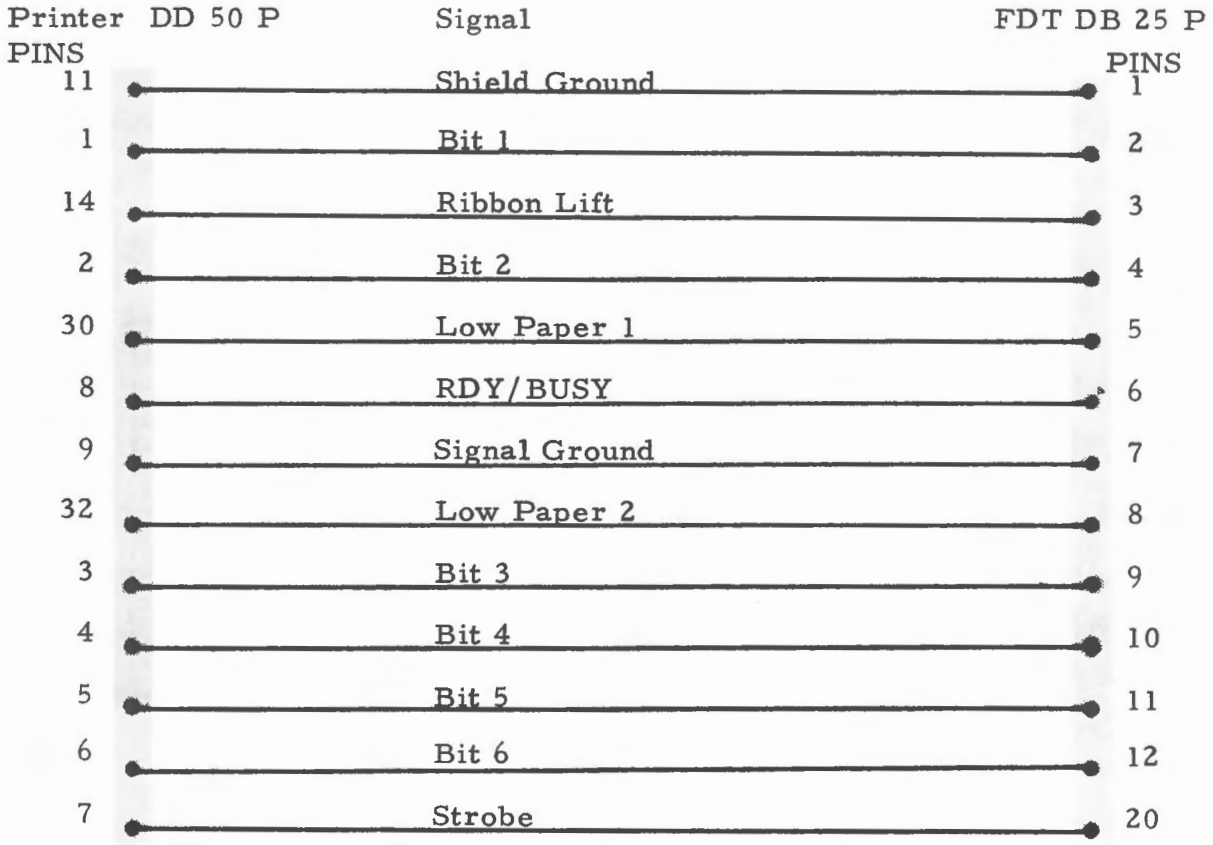
Modem to FDT synchronous or asynchronous half duplex operation



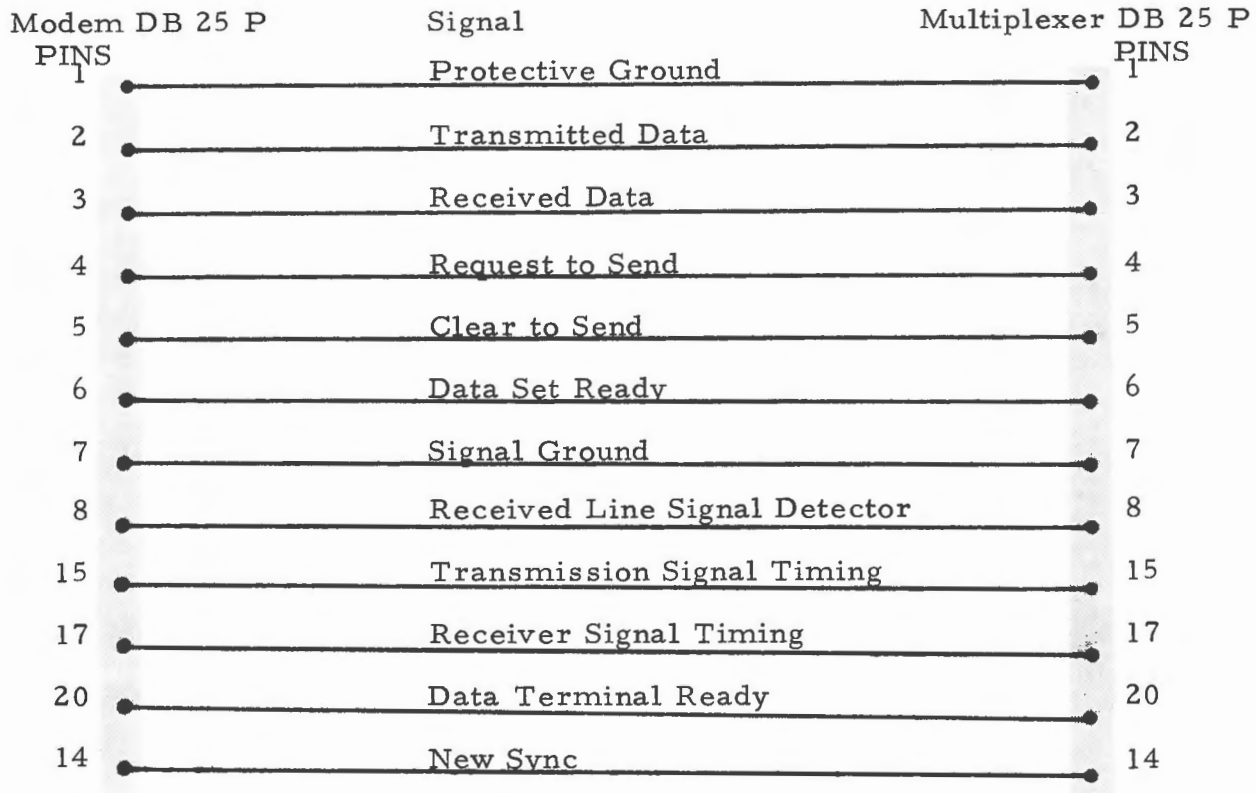
Modem to synchronous or asynchronous controllers full duplex operation.



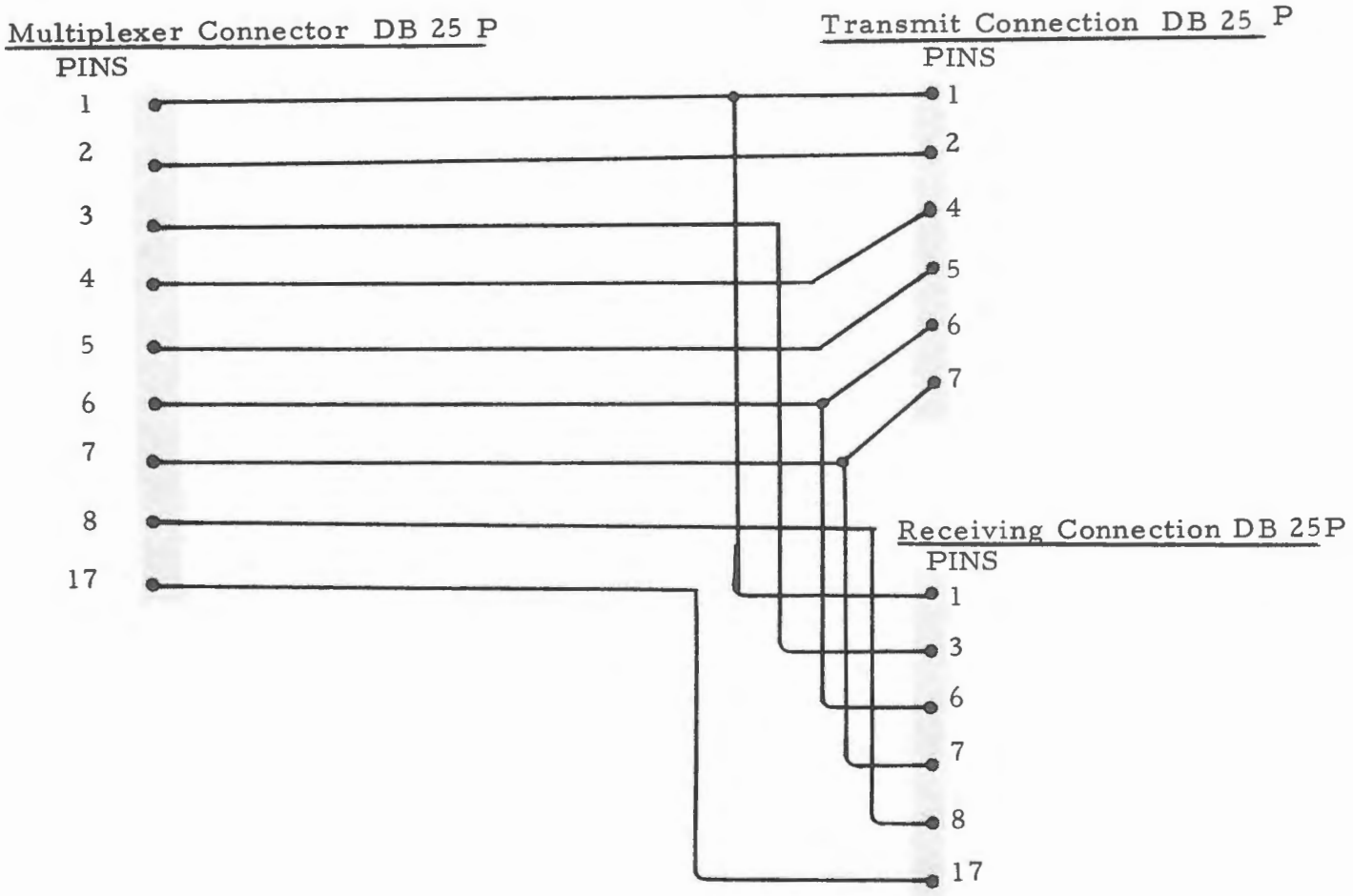
Kleinschmidt Printer to FDT



Modem to Multiplexer, full or half duplex operation. Reference standard I/O cable drawing 001-10-13.



Multiplexer to FDT synchronous or asynchronous controllers. Full duplex operation.



Multiplexer to FDT synchronous or asynchronous controller, HALF Duplex operation.

Multiplexer Connection PINS DB 25 P	Signal	FDT Connections DB 25 P PINS
1	Protective Ground	1
2	Transmitted Data & Data/No Data	2
3	Received Data	3
4	Request to Send	4
5	Clear to Send & STC	5
6	Data Set Ready & Cancel	6
7	Signal Ground	7
8	Received Line Signal Detector	8
17	Receiver Signal Timing	17

NEW DATA ITEM 8

WIRING PLANE SIGNALS AND INTERCONNECTIONS

The following table provides information for the two wiring planes in the SPD 10/20 Display. The Large Plane includes the card slots 10 through 14, all of which have two 86-pin connectors, A and B. The small wiring plane includes all I/O controller slots. The I/O slots have one connector designated C. To locate the routing for a particular signal, the letter is the connector (A, B or C), the next number is the slot and the last number is the connector pin.

LARGE PLANE

Signal	From	To	Signal	From	To
XPD0	B10-74	B11-03	XND0	B10-76	B11-05
XND1	B10-65	B11-07	XPD1	B10-67	B11-09
XPD2	A10-06	B11-11	XND2	A10-04	B11-13
XND3	A10-10	B11-15	XPD3	A10-08	B11-17
XR6	B10-70	B11-19	XR4	B10-60	B11-21
XR2	B10-46	B11-23	XR0	B10-39	B11-25
YND0	B10-54	B11-27	YPD0	B10-52	B11-29
YND1	B10-48	B11-31	YPD1	B10-50	B11-33
YND2	B10-43	B11-35	YPD2	B10-45	B11-37
XND3	B10-49	B11-39	YR6	B10-64	B11-84
YPD3	B10-47	B11-41	YND4	B10-28	B11-43
YPD4	B10-26	B11-45	YND5	B10-22	B11-47
YPD5	B10-24	B11-49	YND6	B10-27	B11-52
YPD6	B10-08	B11-54	YND7	B10-12	B11-56
YPD7	B10-10	B11-58	YR4	B10-63	B11-82
MDSA0	A10-54	A11-53	MDSA1	A10-56	A11-55
MDSA2	A10-58	A11-51	MDSA3	A10-60	A11-59
MDSA4	A10-62	A11-61	MDSA5	A10-64	A11-63
MDSA6	A10-66	A11-65	MDSA7	A10-68	A11-67
MDSA8	A10-70	A11-69	MDSA9	A10-72	A11-71
MDSA10	A10-74	A11-73	MDSA11	A10-76	A11-75
MDSA12	A10-78	A11-77	MDSA13	A10-80	A11-79
MDSA14	A10-82	A11-81	MDSA15	A10-84	A11-83
XR1	B10-42	B11-62	XR3	B10-44	B11-64
XR5	B10-58	B11-66	XR7	B10-68	B11-68
YR1	B10-82	B11-70	YR3	B10-78	B11-72
YR5	B10-72	B11-74	YR7	B10-62	B11-76
YR0	B10-84	B11-78	YR2	B10-80	B11-80

Signal	From	To	Signal	From	To
I0B	A11-03	B10-17	I1B	A11-05	A10-19
I2B	A11-07	A10-21	I3B	A11-09	A10-23
I4B	A11-11	A10-25	I5B	A11-13	A10-27
I6B	A11-15	A10-29	I7B	A11-17	A10-31
I8B	A11-19	A10-33	I9B	A11-21	A10-35
I10B	A11-23	A10-37	I11B	A11-25	A10-39
I12B	A11-27	A10-41	I13B	A11-29	A10-43
I14B	A11-31	A10-45	I15B	A11-33	A10-47
IOA (Z0)	A10-18	A11-04	I1A (Z1)	A10-20	A11-06
I2A (Z2)	A10-22	A11-08	I3A (Z3)	A10-24	A11-10
I4A (Z4)	A10-26	A11-12	I5A (Z5)	A10-28	A11-14
I6A (Z6)	A10-30	A11-16	I7A (Z7)	A10-32	A11-18
I8A (Z8)	A10-34	A11-20	I9A(Z9)	A10-36	A11-22
I10A (10)	A10-38	A11-24	I11A (11)	A10-40	A11-26
I12A (12)	A10-42	A11-28	I13A(13)	A10-44	A11-30
I14A (14)	A10-46	A11-32	I15A (15)	A10-48	A11-34
MDBCM00	A10-55	A12-24	MDBCM01	A10-83	A12-26
MDBCM02	A10-57	A12-22	MDBCM03	A10-81	A12-20
MDBCM04	A10-63	A12-18	MDBCM05	A10-79	A12-16
MDBCM06	A10-65	A12-12	MDBCM07	A10-77	A12-10
MDBCM08	A10-51	A12-08	MDBCM09	A10-53	A12-06
MDBCM10	A10-61	A12-04	MDBCM11	A10-59	A12-05
MDBCM12	A10-75	B12-67	MDBCM13	A10-73	B12-65
MDBCM14	A10-71	B12-63	MDBCM15	A10-69	B12-61
MAR01	A12-25	B10-66	MAR01*	B12-48	B10-14
MAR02	A12-23	B10-53	MAR02*	B12-35	B10-16
MAR03	A12-21	B10-55	MAR03*	B12-28	B10-33
MAR04	A12-27	A10-07	MAR04*	B12-27	A10-03
MAR05	A12-29	A10-09	MAR05*	B12-21	A10-05
MAR06	A12-31	B10-59	MAR06*	B12-17	B10-69
MAR07	A12-11	B10-75	MAR07*	B12-15	B10-71
MAR08	A12-13	B10-61	MAR08*	B12-34	B10-73
MAR09	A12-15	B10-51	MAR09*	B12-50	B10-41
MAR10	A12-09	B10-31	MAR10*	B12-52	B10-37
MAR11	A12-07	B10-18	MAR11*	B12-36	B10-20
CCG56	A14-41	B14-38	TURL0	B14-22	B14-11
TURL1	B14-26	B14-08	TURL2	B14-28	B14-06
TURL3	B14-24	B14-04	TURL4	B14-32	B14-07
CTU99	A14-36	B14-39	VPS	A14-79	B14-62
CPI88	A14-38	A14-16	CPI88	A14-16	B13-62
CPI88N	A14-42	A14-14	CPI33	A14-06	A14-32
CPI33	A14-32	B14-72	CPI11	A14-34	A14-08
CPI22	A14-26	A14-12	CPI44	A14-28	A14-10
CPI55	A14-35	A14-04	CPI66	A14-37	A14-17

Signal	From	To	Signal	From	To
MDR05*	B13-42	B12-25	MDR06*	B13-65	B12-37
	B12-25	B10-35		B12-37	B10-23
MDR07*	B13-59	B12-49	MDR08*	A13-05	A12-64
	B12-49	B10-25		A12-64	B10-56
MDR09*	A13-19	A12-66	MDR10*	B13-82	A12-68
	A12-66	B10-57		A12-68	B10-79
MDR11*	A13-66	A12-70	MDR12*	A13-60	A12-72
	A12-70	B10-77		A12-72	B10-83
MDR13*	A13-68	A12-74	MDR14*	A13-64	A12-76
	A12-74	B10-81		A12-76	A10-11
MDR15*	A13-77	B12-57	TOPSEC	A13-04	B12-62
	B12-57	A10-12	TCD20	A13-21	B12-71
MARCUR	A13-75	B12-76	PWRUPI	B13-66	B10-17
CPT02	A14-45	B13-04	CPT03	A14-49	B13-38
CPT04	A14-24	A13-15	CPT05	A14-51	A13-34
CPT07	A14-47	A13-06	CPT08	A14-56	A13-03
	B10-21	A13-06	CPT09	A14-62	A13-36
CPT10	A14-50	B13-36		A13-36	B10-15
	B13-36	B10-11	CPT11	A14-58	A13-10
CPT14	B14-56	A14-46	CPT16	A14-48	A13-23
	A14-46	A13-81		A13-23	B10-13
CPT17	A14-63	A13-40	CPT19	A14-53	B13-58
	A13-40	B10-09	CPT20	A14-60	B13-50
REFREQ	B14-54	B13-74	REFREQ*	B14-52	B13-64
REFSIG	B14-49	B13-12	REFSIG*	B14-50	B13-40
TURT4	A14-66	B13-18	RTC	A14-77	B13-06
RMAAABI	B14-21	B13-52	CPT13	A14-57	B14-16
CONT14	B14-18	A13-52		B14-16	B13-14
OTB00	A12-84	B14-13	OTB01	A12-50	B14-15
OTB02	A12-48	B14-17	OTB03	A12-46	B14-19
OTB04	A12-44	B14-09	FUNC00	B13-45	B14-44
FUNC01	B13-47	B14-05	FUNC02	B13-63	B14-03
FUNC03	B13-57	B14-20	RESET	B13-56	B14-34
CPI23	A14-20	B10-19	WAIT	B10-07	B13-10
CPT01	A11-84	A14-52	IDI	B14-40	B14-85
+5VDC	A10-67	A10-02	-5VDC	A11-42	B14-69
-14VDC	A11-37	A11-38		A11-41	A11-42
	A11-38	B14-45		B14-69	B14-70
	B14-45	B14-46	+14VDC	B10-29	B10-30
+25VDC	B10-05	B10-06	+5VDC	A10-01	B10-01
	B10-06	B14-73		A11-01	B11-01
	B14-73	B14-74		A12-01	B12-01
VIDIO	B14-76	B14-59		A13-01	A13-01
VSYNC	B14-78	B14-61		A14-01	B14-01
HSYNC	B14-80	B14-63	TURT1	A14-54	A10-49

Signal	From	To	Signal	From	To
CPI77	A14-43	A14-19	TUD908	A14-44	A14-71
AABCC00	B12-04	A14-72	AABCC01	B12-06	A14-73
AABCC02	B12-08	A14-75	AABCC03	B12-10	A14-68
AABCC04	B12-12	A14-70	AABCC05	B12-24	A14-74
AABCL06	B12-14	B14-25	AABCL07	B12-20	B14-27
AABCL08	B12-16	B14-14	AABCL09	B12-26	B14-23
AABCL10	B12-18	B14-64	CSI02	B12-68	A14-78
CRG00	A10-52	A14-64	CRG00	A11-82	A10-52
ARB00	A12-65	B14-37	ARB01	A12-63	B14-35
ARB02	A12-53	B14-60	ARB03	A12-51	B14-33
ARB04	A12-61	B14-31	ARB05	A12-49	B14-29
ARB06	A12-59	B14-36	ARB07	A12-60	A14-81
CPT13	A14-57	B14-16	OPDG02I	A13-84	A12-33
OPDG03I	A13-82	B12-54	OPDG04I	A13-80	A12-58
OPDG05I	A13-78	B12-56	STRBBYTE	A13-41	A12-03
OPD26I	A13-83	A12-78	OPR04	A13-73	B12-69
STRBPCRI	A13-28	B12-33	STRBLIR	A13-33	B12-79
STRBCHR	A13-31	B12-81	AARCUR	A13-58	B12-70
MEMSTRB	A13-27	B12-75	ACRMDB	A13-43	B12-82
ACRJIN	A13-24	A12-42	ACRKIN	A13-26	A12-47
STRBMDR	A13-45	B12-77	AAR/MAB	B13-78	A12-28
STRBACRL	B13-72	A12-52	STRBACRM	B13-70	A12-40
STRBMAR	B13-34	A12-30	EXTW	B13-48	B12-83
EXTFI	B13-54	B12-80	LOW/AAB	A13-46	B12-13
MDR/AABM	A13-42	B12-07	MDRAAB	A13-44	B12-09
PCR/AABM	A13-48	B12-19	PCR/AAB9	A13-50	B12-29
PCR/AAB	A13-30	B12-11	CURAAB	A13-17	B12-05
MAR/AAB	B13-32	B12-03	+2AAU	A13-13	B12-58
+1/AAU	B13-44	B12-59	+4/AAU	A13-16	B12-60
-1/AAUL	A13-11	B12-30	RFBYPASS	B13-80	B12-73
AAR/AAU	A13-09	B12-32	STRBAAR	B13-60	B12-31
ACRARU	A13-20	B12-78	ACR/ARU	A13-18	A12-54
MDR/ARBI	A13-38	A12-82	MDR*ARB	A13-22	A12-80
LOW/ARBM	A13-62	A12-56	IOARB	A13-12	A12-67
STRBCSR	A13-14	B12-74	AAU/CSR	A13-08	B12-66
ACR/ARB	A13-32	A12-62	MABSP02	B13-03	A12-57
MABSP03	B13-08	A12-41	MABSP04	B13-20	A12-39
MABSP05	B13-05	A12-37	MABSP06	B13-73	A12-43
MABSP07	B13-75	A12-36	MRBSP08	B13-77	A12-34
MABSP09	B13-67	A12-32	MABSP10	B13-69	A12-35
MABSP	B13-73	A12-45	AARMDB	A13-29	B12-72
MDR00*	A13-70	B12-46	MDR02*	A13-74	B12-38
	B12-46	B10-40		B12-38	B10-34
MDR03*	A13-76	B12-40	MDR04*	B13-43	B12-23
	B12-40	B10-36		B12-23	B10-32

SMALL PLANE

Signal	From	To	Signal	From	To
OTB00	A12-84	C05-03	INB00	A12-77	C04-04
	B14-13	C04-03		A12-77	C05-04
OTB01	A12-50	C05-05	INB01	A12-79	C04-06
	B14-15	C04-05		A12-79	C05-06
OTB02	A12-48	C05-07	INB02	A12-81	C04-08
	B14-17	C04-07		A12-81	C05-08
OTB03	A12-46	C05-09	INB03	A12-83	C04-10
	B14-19	C04-09		A12-83	C05-10
OTB04	A12-44	C05-11	INB04	A12-69	C04-12
	B14-09	C04-11		A12-69	C05-12
OTB05	B12-55	C04-13	INB05	A12-71	C04-14
	B12-55	C05-13		A12-71	C05-14
OTB06	B12-53	C04-15	INB06	A12-73	C04-16
	B12-53	C05-15		A12-73	C05-16
OTB07	B12-51	C04-17	INB07	A12-75	C04-18
	B12-51	C05-17		A12-75	C05-18
TYP00	A13-07	C04-19	FUNC00	B13-45	C04-20
	A13-07	C05-19		B14-44	C05-20
TYP01	A13-25	C04-21	FUNC01	B13-47	C04-22
	A13-25	C05-21		B14-05	C05-22
ATTENTION	B13-61	C04-23	FUNC02	B13-63	C04-24
	B13-61	C05-23		B14-03	C05-24
FUNC03	B13-57	C04-26	AKDRTC	B13-76	C04-27
	B14-20	C05-26		B13-76	C05-27
+14V	A13-37	C05-75	CONT00	A13-63	C01-28
CONT01	A13-61	C02-28	CONT02	A13-59	C03-28
CONT03	A13-65	C04-28	CONT04	A13-67	C05-28
CONT05	A13-69	C06-28	CONT06	A13-71	C07-28
BOOT	B13-68	C04-29	INT0	B13-41	C01-30
	B13-68	C05-29	INT1	B13-37	C02-30
INT2	B13-35	C03-30	INT3	B13-27	C04-30
INT4	B13-39	C05-30	INT5	B13-33	C06-30
INT6	B13-31	C07-30	INTSELIN	B13-16	C01-31
INTSELOUT	C04-32	C05-31	CPT18N	A14-33	C03-35
CPT18N	A14-33	C06-35	RET	B13-86	C03-86
RET	B13-86	C06-86	CPT08N	A14-31	C02-36
CPT08N	A14-31	C07-36	RET	B12-85	C02-85
RET	B12-85	C07-85	TURT4	B13-18	C02-37
TURT4	A14-66	C07-37	RET	B12-86	C02-86
RET	B12-86	C07-86	RESET	B13-56	C04-25
RESET	B14-34	C05-25	RET	B14-85	C04-85
RET	B14-85	C05-85			

Signal	From	To	Signal	From	To
CPT13N	A14-39	C04-33	CPT02N	A14-22	C03-34
RET	B14-86	C04-86	RET	B13-85	C03-85
CPT13N	A14-39	C05-33	CPT02N	A14-22	C06-34
RET	B14-86	C05-86	RET	B13-85	C06-85

NEW DATA ITEM 9

INPUT/OUTPUT CONNECTOR ARRANGEMENT

Most cables, once installed, remain in the installed position while the Terminal remains in the original position. This is not true of the 50-pin Program Loading position. Formerly, the 50-pin connector was located on the I/O connector panel adjacent to the eighth 25-pin connector. (Figure 1 provides an overall bottom view.) For convenience the connector has been relocated to the right side of the Terminal as illustrated in Figure 2. With the relocated connector, it is not longer necessary to tilt the Terminal forward to insert the loader cable.

The same restriction was also true of the BOOT button which was located on the bottom of the Terminal. The BOOT button puts the BOOT controller into the BOOT condition and is easily reached by the operator. The BOOT button is co-located with the 50-pin connector (see Figure 2).

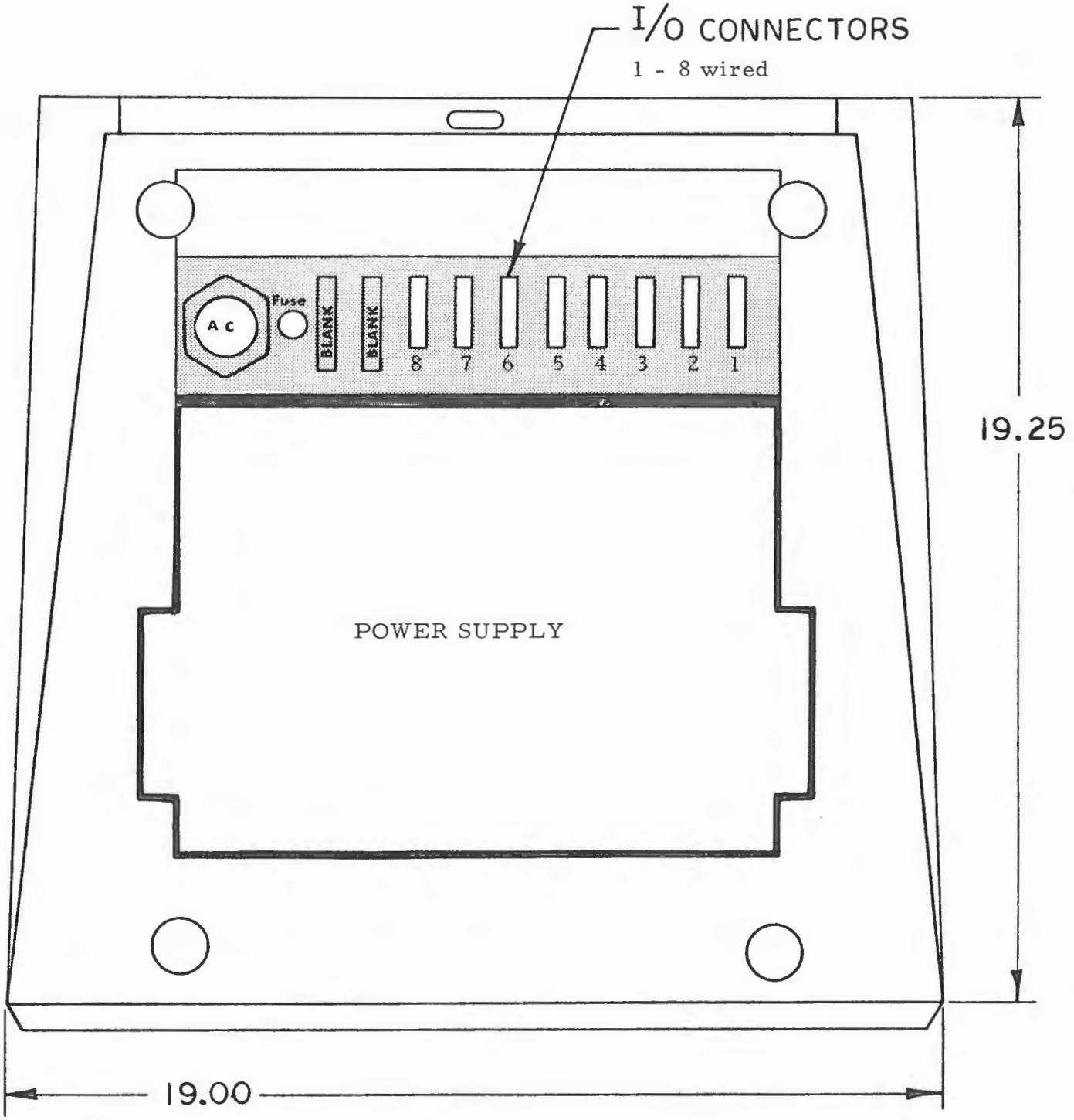


Figure 1. BOTTOM VIEW

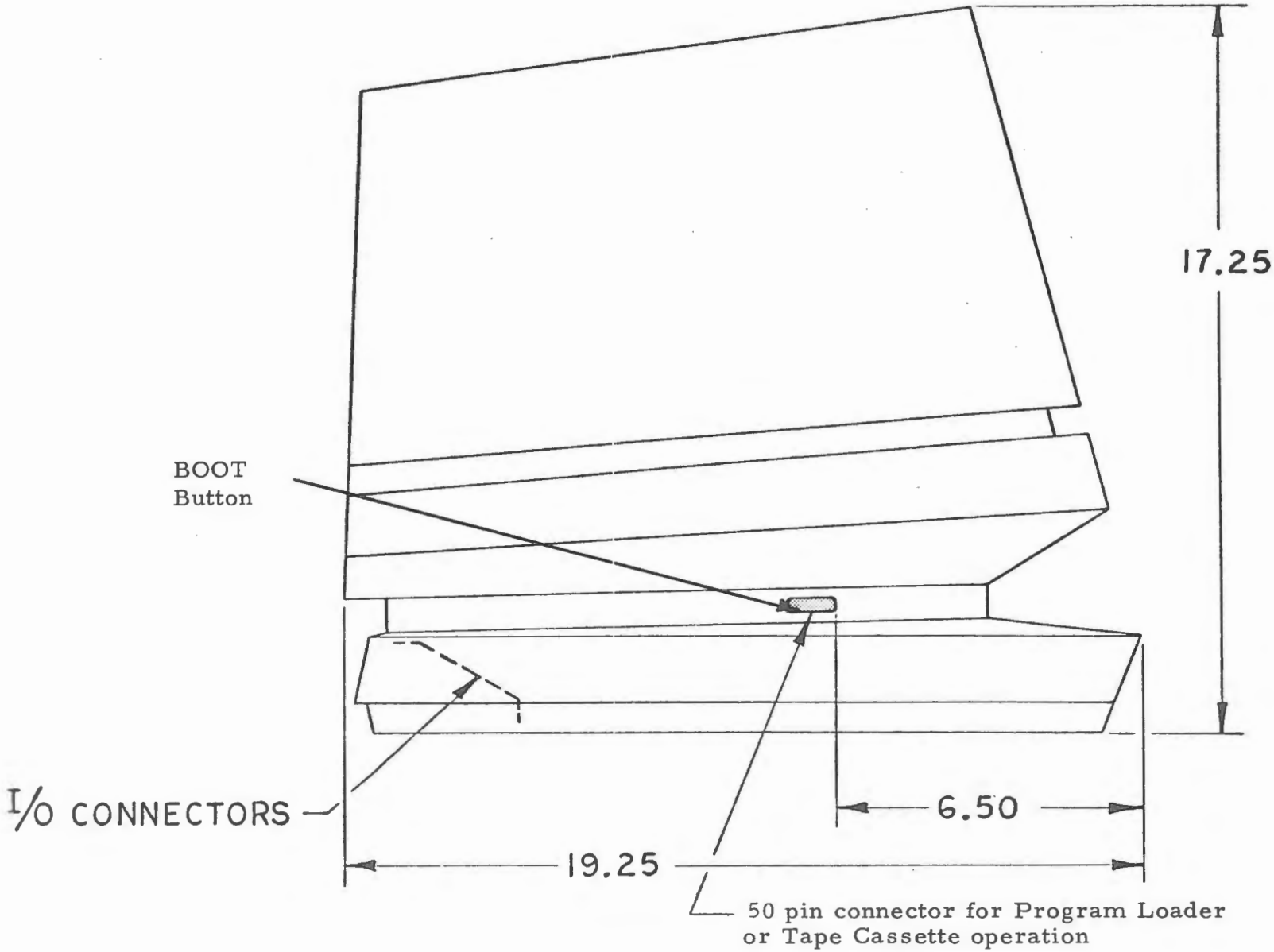
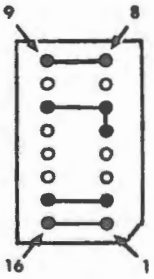


Figure 2. SIDE VIEW

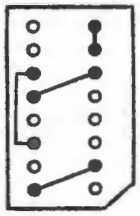
OPTION BLOCKS

The following option blocks supplement those found in Appendix B.

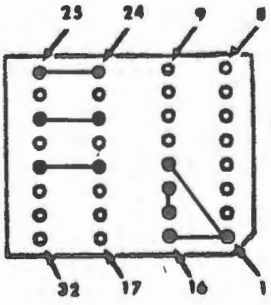
ASYNCHRONOUS CONTROLLER



Part NO.	STB NO.	Function
	26	Multiplexer Operation

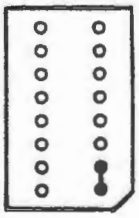


001-11-01-790	42	Multiplexer to Asynchronous Modem

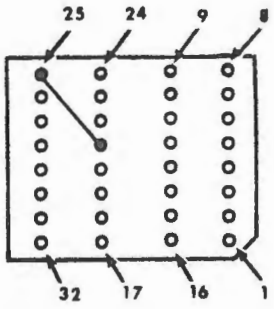


001-11-02-729	65/66	No Parity Check or Generate - Internal Clock 1200 Baud

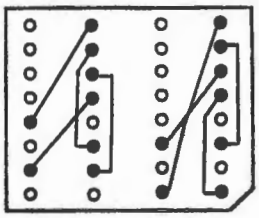
BOOT CONTROLLER



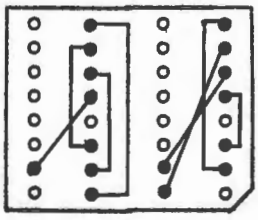
001-11-01-791	39	Inhibit Timer



Part NO.	STB NO.	Function
001-11-02-730	17/18	Inhibit Address



001-11-02-731	25/26	Character = (3D) 16



001-11-02-732	43/44 or 34/35 or 52/53	Character = (1E) 16

REVISED DATA

5.5 REFRESH MODULE TIMING UNIT (BOAC)

General

The Refresh Module Timing Unit (RMTU) circuitry is modified to add functions to the circuit board which previously were performed on two additional boards. One is the addition of the system oscillator to the RMTU board, and the other is circuit modification which enables the RMTU to perform a split screen function, thereby eliminating the I/O circuit board designed for split screen signla processing. Schematic 009-14-01 Rev A schematically illustrates the added circuitry. The following description applies to the operational difference between the standard RMTU and BOAC RMTU.

Theory of Operation

The System 12/6 MHz oscillator is drawn on schematic 009-14-01, sheet 12, Refresh Module Line Selection. The function of the oscillator is identical to that of Paragraph 5.7, Page 5-76, SPD 10/20 Technical Manual. The former oscillator used element M1 connected as an inverter. The 009 version uses inverters (Texas Instruments 7404) M109. The output signal OSC is fed to sheet 8 circuit M106. The former clock input pin A84 is maintained as a distribution point for the 12.6 MHz signal. Also on sheet 8, the system power UP reset signal is incorporated; formerly the signal was generated on the TPU control board. AND gate M102 is enabled by the

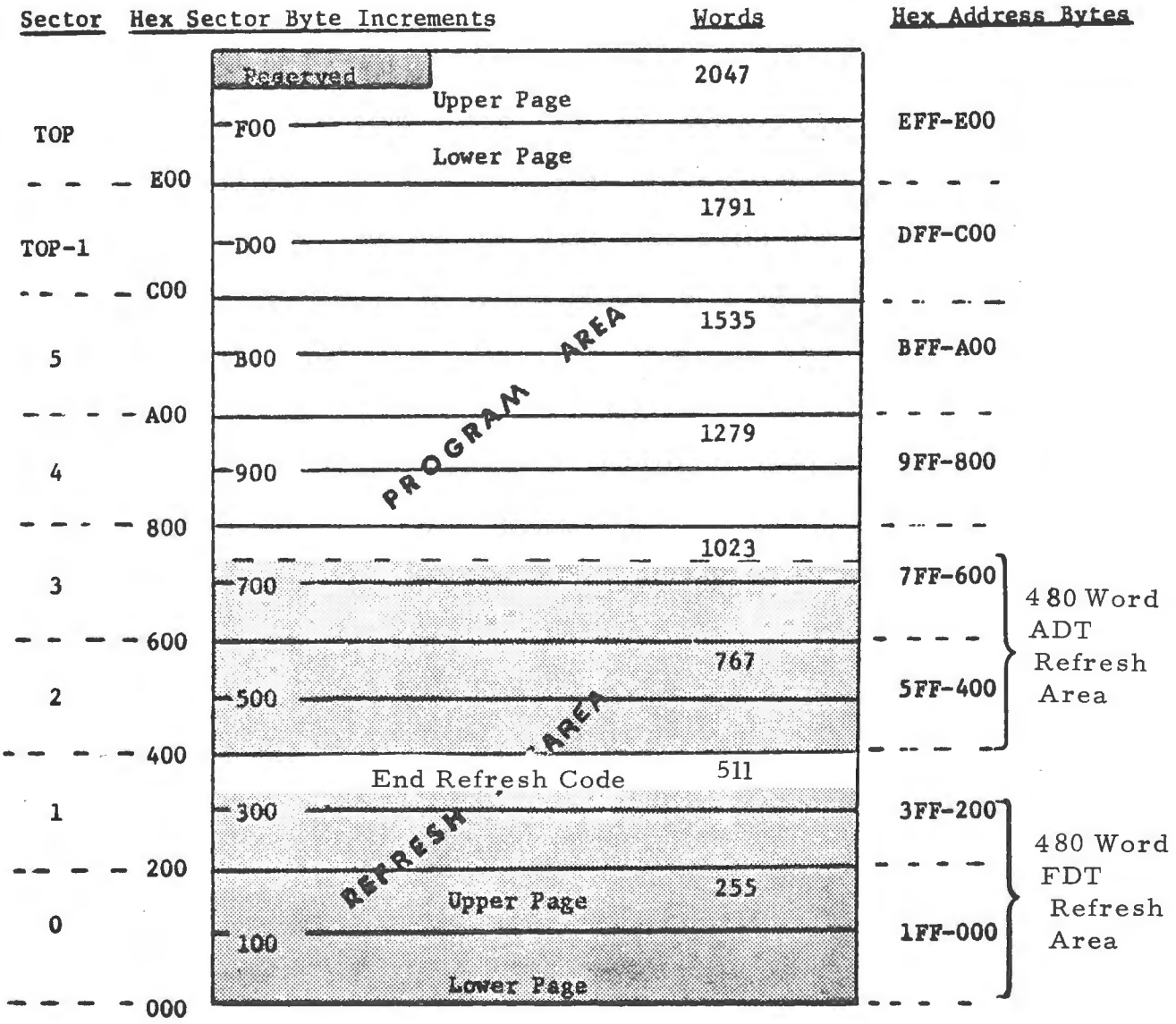


Figure 1. 2K Core Memory Layout Illustrating FDT and ADT Refresh Area For Alternate Line Operation.

power UP signal from the power supply ANDed with a sequencer signal from gate M54. The true condition results in a high signal at pin 1, inverted at M108 and distributed throughout the Terminal at connector pin A79.

Alternate line operation involves signal processing which is utilized when an auxiliary terminal is being provided with display data, utilizing the Freestanding Display Terminal for computation and refresh. Figure 1 illustrates the dedicated refresh areas for FDT, ADT alternate line operation. The dedicated area for the FDT refresh function starts at word 0_{10} and is contiguous through word $479_{(10)}$. Word address $480_{(10)}$ is reserved for the End of Refresh code. The ADT refresh area starts at word location $512_{(10)}$ and is contiguous through word $991_{(10)}$. Table 1 lists the actual allocation of words per display line. The 15 line presentation is refreshed by alternating from one complete FDT line to one complete ADT line until the full refresh has been accomplished. The starting position can be moved down the screen as many as seven lines using the TPU C I/O command. Such movement does not change the refresh data location, but does limit the number of displayable lines. The end of display code is decoded only in the FDT refresh area; this feature allows addresses greater than the end of display to contain any code without changing the presentation in the FTD display. If the presentation is to start on the normal line and end after 14 lines, the End of Refresh code is located at word address $448_{(10)}$.

The control/start and last line functions are found on schematic 009-14-01. This circuit functions as that illustrated by a 005-14-01 schematic with two minor exceptions. The REFRESH signal from M45 pin 11, which formerly went only to the STD, now must be shared with the ATD, and the signal wire BRIGHT B* has been added. Also from the $\overline{Q}$ side of M45, a control signal called RMGCL is taped from pin 10. This signal performs a reset

*NOTE

For schematic interpretation, FTD signals are labeled A and ATD signals are labeled B.

Table 1. Refresh, Line/Word Allocation FDT and ADT

Address of First Word of Line$_{(10)}$			Address of Last Word of Line$_{(10)}$
0	FDT Line	1	31
32	FDT Line	2	63
64	FDT Line	3	95
96	FDT Line	4	127
128	FDT Line	5	159
160	FDT Line	6	191
192	FDT Line	7	223
224	FDT Line	8	255
256	FDT Line	9	287
288	FDT Line	10	319
320	FDT Line	11	351
352	FDT Line	12	383
384	FDT Line	13	415
416	FDT Line	14	447
448	FDT Line	15	479
480	Bytes 960 and 961 used for EOD		511
512	ADT Line	1	543
544	ADT Line	2	575
576	ADT Line	3	607
608	ADT Line	4	639
640	ADT Line	5	671
672	ADT Line	6	703
704	ADT Line	7	735
736	ADT Line	8	767
768	ADT Line	9	799
800	ADT Line	10	831
832	ADT Line	11	863
864	ADT Line	12	895
896	ADT Line	13	927
928	ADT Line	14	959
960	ADT Line	15	991

function when in vectors and is part of the enabling circuit for an End Display signal. The refresh signals A and B are fed to the video circuits on sheet 6 where they become an enabling leg of AND gates M5 BRIGHT B and BRIGHT A respectively. The three signals necessary for each display are outputted from this circuit. The VIDEO B feeds through OR gate M7 (used as an inverter) and out to pin B71. Horizontal sync B is outputted from pin B65 and Vertical sync B is outputted from pin B67. The three A signals are VIDEO A at pin B76, Horizontal sync A at pin B80 and Vertical sync A at pin B78. Other enabling signals at M5 (A and B) are the Horizontal blanking, character Video decode and TURL0. The signal TURL0 is fed to AND gates M5 from the line counter, sheet 4, and is the signal which switches from ADT to FDT by alternately enabling M5. TURL0 is a carry function of line comparitor CLA00-03 where the start line address from the TPU is compared to the RMTU timing unit register. The summation of the inputs A and B are fed to the TPU Auxiliary Arithmetic Bus as the line address and the same signals are ANDed at M/5 to provide the start display signal. Gate M42 is used as a simple inverter which provides the BRIGHT B (VIDEO) signal as a function of the TURL0 state 0 or 1. With TURL0 high, AND gate BRIGHT A is enabled and when TURL0 is low, BRIGHT B is enabled. Signal ENDIGA is an AND gate M8, sheet 5, where the state control reset conditions are ANDed with TURL0, signaling the FDT End Display limit.

The Refresh signal routed to sheet 3 state control is ORed with H SYNC at M87. The output signal of M87 is the vector reset to pin 3, M33, and is fed to pin 10, M8, End Display signal, sheet 5. The output of M8 is ANDed with the decoded count of 74 at M73 and the resulting signal resets the display flip flop M31 on sheet 2, which resets the Refresh flip flops.

Vertical sync timing is decoded from the first two bits of the timing unit register, sheet 9. Component M106, the enabling input, is a count of 1. The output signal is fed to sheet 14 as the clocking input to M86, the V Sync flip flop. The signal V Sync A and V Sync B are enabled by the vertical line and segment gating.

Horizontal Sync for Displays A and B (FDT and ADT, respectively) is generated on sheet 11, flip flops H Sync and H Blank (M91). Low frequency divider M94 provides the cursor blink rate for the hardware blink option. If software is used to blink the cursor, STB 105 pins 9 and 12 are left open.

The BOAC character set used is different from the standard INCOTERM set. The display characters are stored in a Read Only Memory; therefore, a change in character font or symbols is accomplished by changing the Read Only Memory. The alphanumerics and special characters displayable on the BOAC display are as follows:

@ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

0 1 2 3 4 5 6 7 8 9 SP ! $ & , ( ) * + - . / : ; < = > ?

Access to the SP location results in no character presentation, in effect, a space.

5.6 TERMINAL SYSTEM POWER SUPPLY

General - The 010 Model Power Supply supersedes the 001 Model at the phase-in point of Terminal #250 and above. The revised power supply maintains external physical characteristics similar to the 001 Model and is operated and fastened at the same locations within the Terminal (see Figure 1). Functionally, the supplies are compatible; however, the power wiring connections are different and therefore not interchangeable. In addition to the 001 Terminal voltages, the revised supply provides a +24 volt line for the display monitor. The dc to dc conversion rate is performed at a higher frequency which completely eliminates audio hum. As illustrated in Figure 1, the fuses have also been eliminated. Short circuit and overvoltage conditions are electronically fused within the supply. Figure 2 illustrates the ten basic functional blocks described as follows:

1. Input and Isolation Transformer - serves the dual purpose of isolating the ac input from the system ground, and transforms the ac 115 or 230 V input (via Taps) to the required working voltage.
2. Fullwave Bridge - converts the transformed input ac into a dc voltage.
3. Input Filter - filters the dc input.
4. Switching Regulator - regulates the unregulated input to a predetermined level. The regulator is regulated with respect to the +5V output.
5. Square Wave Generator - generates a square wave of a predetermined frequency (approximately 40 KC).
6. Driver Circuitry - amplifies the input square wave to a level adequate for driving the dc-dc converter.
7. The dc-dc converter converts the dc output of the switching regulator to a square wave. Frequency is dictated by the square wave generator. This square wave is then transformed by the dc-dc converter transformer to the required output levels where it is rectified and filtered to provide the system dc power.

8 & 9. The +25V and +14V output series regulators provide the required temperature compensation and regulation.

10. The required turn-on, turn-off, and failure sensing is provided by the power-up circuitry.

Theory of Operation

Figure 3 illustrates the internal layout of the power supply, locating the plug in circuit boards A and B, plugs, jacks and adjustment locations. Referring to Figure 2, a simplified block diagram, and schematic 010-13-01, the ac input transformer provides multiple tap input positions. The transformer (T1) is physically wound with two separate primary windings, each of which can be jumpered at specific pins and accept a range of voltages from 105 volts RMS to 250 volts RMS. The in phase voltage additions are as listed on the schematic. The secondary winding is attached to the ac input of full wave bridge rectifier CR1. The negative potential of the rectifier is grounded to the chassis and the positive side is capacitor filtered by C1. R60 provides a bleedoff path for C1. The +dc rectified voltage is in the range of from 65 to 95 V dc.

The rectified input voltage is routed to the several operating circuits where it is individually zener regulated to the proper level for that particular circuit. At connection J6-C the rectified dc is used as the anode potential on silicone controlled rectifier S1 through R17, a 15 KΩ1 watt resistor. The voltage is also applied across the combination R18 and VR4. VR4 provides zener regulation at 5.1 volts for VCC application in the multivibrator (Q6, 7, 8 and 9) and push pull transformer driver circuit. Also at the input, the potential is applied across R1 and VR1 resulting in a zener regulated +24 volts for application to the input voltage regulator M1 pin 12. At J5-6 the potential is routed to the power up circuitry (Q20) and at J5-L the voltage is applied across the combination R28 and VR6. The zener regulation of VR6 (+4.7 volts) is applied to the base of Q14 as a reference voltage for the power up voltage comparator Q14 and Q15.

The integrated circuits M1, M3 and M4 are Fairchild μA723C voltage regulators. Some inherent features are:

1. Temperature compensated reference amplifier
2. Error Amplifier

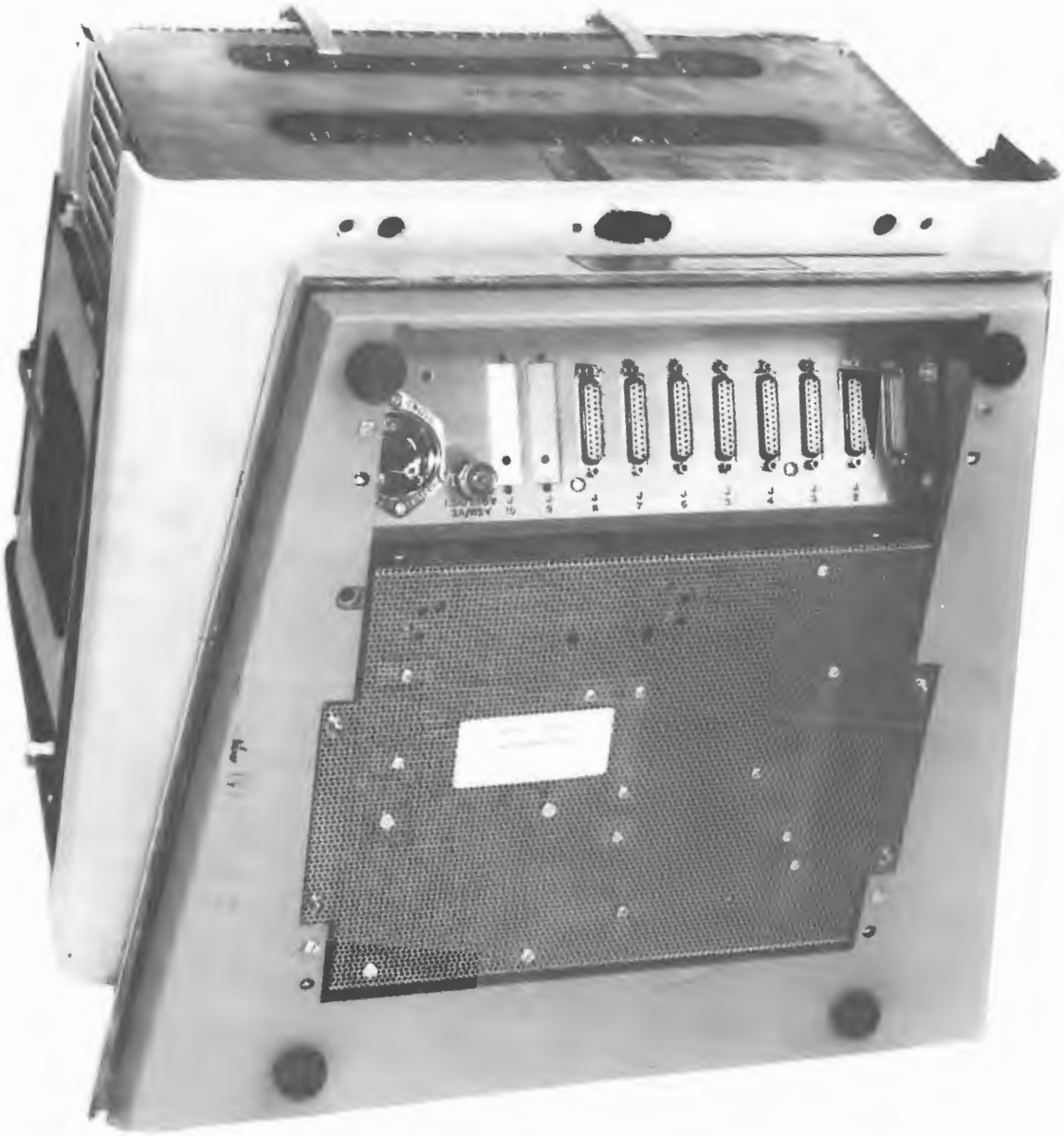


Figure 1. Bottom View
Model 010 Terminal System Power Supply

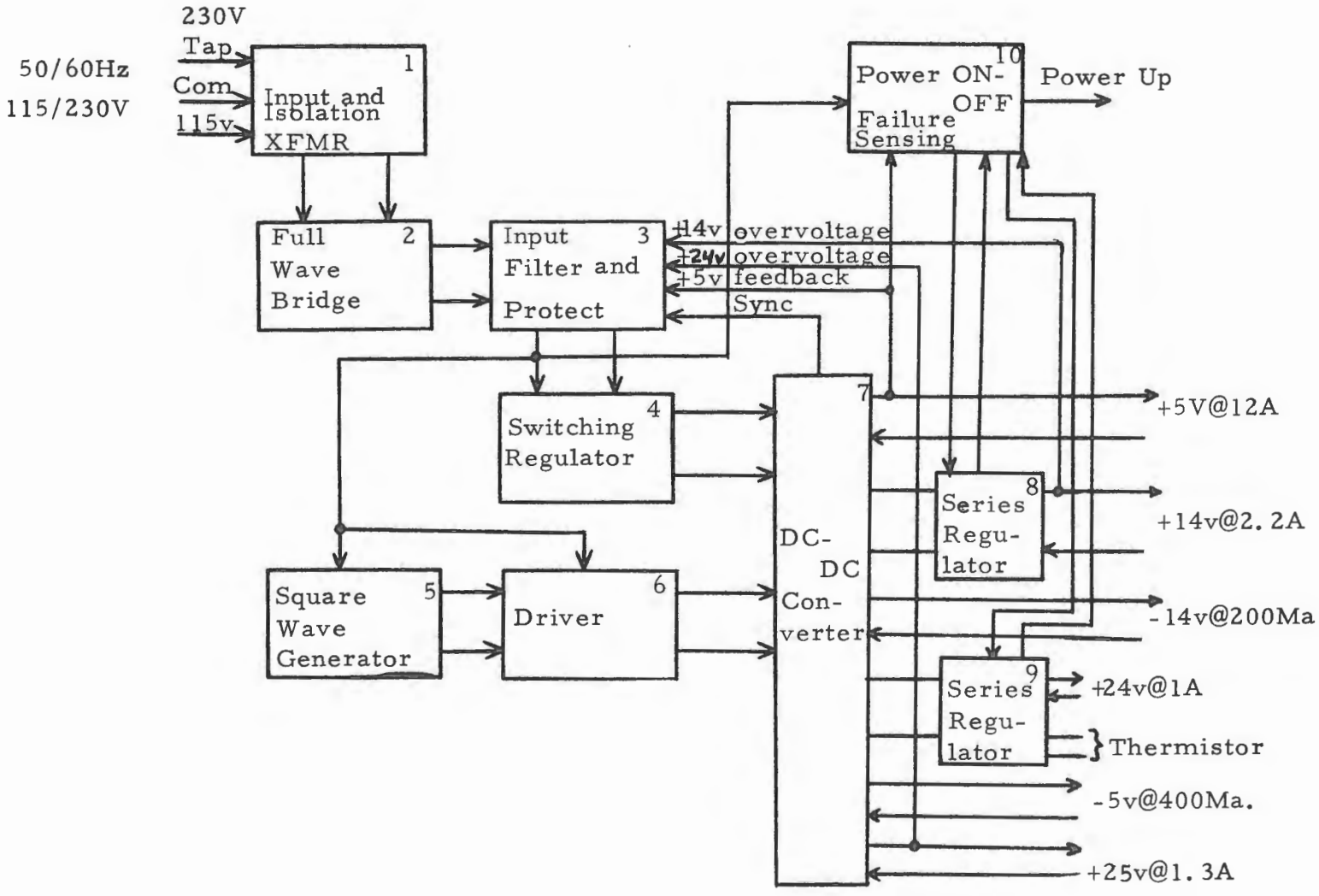


Figure 2. Power Supply Block Diagram

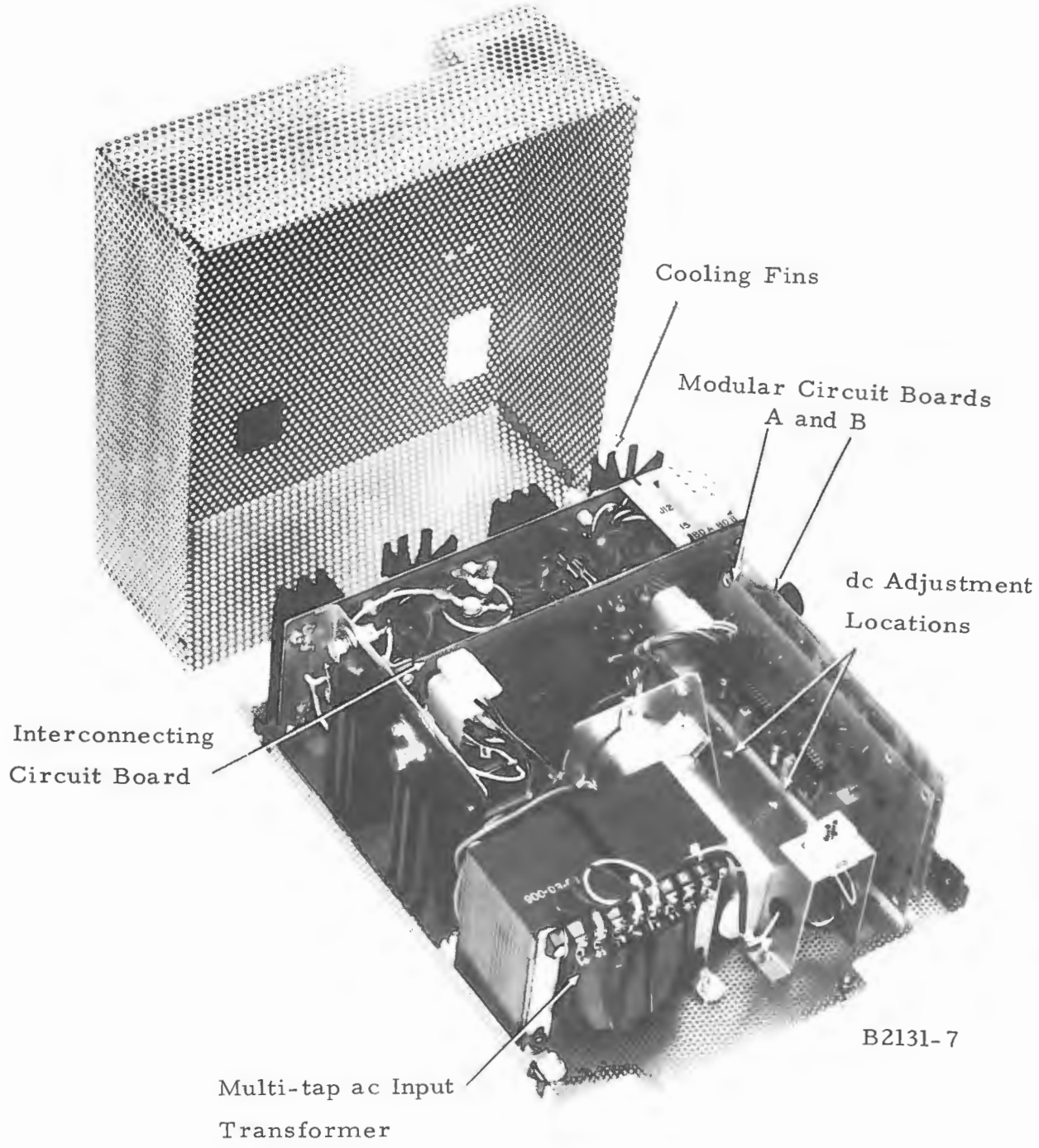


Figure 3. Internal View, Terminal System Power Supply

3. Series power pass transistor and current limiting circuitry
4. Adjustable current limiting and remote shutdown.

The input regulator, M1, performs an input regulation with reference to the output +5 volts. When the +5 volt potential rises above the +5 volt threshold, series transistor Q1 open circuits the input line, thus opening the power source to transformer T3 centertap. When the +5 volts is less than threshold, Q1 closes. The waveform resulting from this operation is a pulse width wave as a function of the +5 volt condition. Operating frequency of the input regulator is synchronized with the transformation rate. Point B on the secondary of T3 is fed back to the input regulator. The signal is taken prior to -5 volt rectification and is fed back through coupling capacitor C21. The input regulator can be adjusted at R9 on circuit board B. Since variations caused in primary input operation effect all secondary voltages, adjustment R9 causes a change in all secondary dc levels. R9 should be adjusted using the +5 volt level as a reference point. (The accuracy of the adjustment depends on the accuracy of the measuring device, ie a digital reading of at least two decimal points is desirable.)

Fault conditions are detected at the input circuit for both over-voltage and over current conditions. The B board inputs C and D are a result of overvoltage dc conditions detected at the output. If the +14 volt output line rises to a value higher than the zener threshold of VR3 (15 volts), VR3 conducts, which creates a voltage drop across R57 and the signal at point C is fed to diode CR3. The positive potential on the anode of CR3 causes it to conduct and the resulting drop across R14 causes the silicone controlled rectifier to conduct (switch to ground). With S1 shorted, the ground reference level is applied to M1 pin 13 through CR10 and all outputs are disabled when regulator M1 causes series transistor Q1 to open.

The input at point D causes a similar reaction. When the +24 volt line rises above the zener threshold of VR2 (27 volts) the resulting voltage is applied across divider R61 and R14, thus firing S1. Of particular interest to the +24 volt overvoltage protect is the fact previously mentioned that all the secondaries react similarly; therefore, if the +5 volt voltage were to increase,

the +24 would also increase. Observing the schematic VR2 functionally serves as the overvoltage protect for the +5, -14, -5 and +24 volt secondaries (the +14 and +25 are individually protected and regulated). A third input to the SCR (S1) is the result of overcurrent detection by Q4. R13 A and B are two 0.16Ω resistors in parallel which is equivalent to 0.08Ω. The resistance is in series with the center tap power lead and if over current is drawn, the voltage drop across R13 biases Q4 on, and the IR drop across R14 fires S1. The circuit from pins J5-A to J5-B provides a brief delay time during which Q4 is held inoperative. This circuit assures that during the initial power up, the capacitor charging current will not be interpreted by Q4 as a fault condition. Any of the above conditions which cause the silicone controlled rectifier to activate result in curcuit protection without fusing. However, when the fault is removed, the supply will still be inoperative. When S1 has been fired, the only way to regain proper circuit operation is to remove the anode supply voltage (the SCR is effectively a solid state thyratron). Circuit operation is resumed by momentarily removing ac power with the Terminal ON/OFF switch.

The transformer driver circuitry is also located on the B circuit board. When power is initially applied, VR4 supplies +5.1 volts Vcc to the driver circuitry. Q7 and Q9 are configured as a free running astable multivibrator. Transistors Q6 and Q8 insure that the multivibrator will restart every time power down occurs. If, upon power up, both Q7 and Q9 were to be saturated at the same time, Q6 and Q8 operate to normalize the operation. The frequency of operation is 40 KHz which is applied from the collector of Q9 to the clock input of M2, a low power flip flop. M2 has the preset pin tied to Vcc and clear tied to ground resulting in a toggle operation. The toggle action of M2 results in outputs Q and $\overline{Q}$ at 20 KHz (40/2) which are 180 degrees out of phase. The outputs are passed through diode switches CR23 and CR28 on low cycles. The low signals are capacitor coupled to the cathode base connection of Q10 and 11 respectively. The resulting bias operates the Q10-Q11 pair and therefore the Q22-Q23 pair as push pull

circuits driving the primary of T2. T2 center tap power is provided by the regulated dc input line which is approximately +45 volts dc at the + side of C3. Primary current limiting is accomplished by R25, a 220Ω resistor in series with the input dc power wire. The alternations produced in the T2 secondary drive the base of Q12 and Q13. On 180 degree cycles the push pull effect causes alternations in the primary winding of T3. Current limiting in the T3 primary drive curcuit is provided only by the dc resistance of the winding and internal resistance of the power transistors. The secondary windings of T3 are each full wave rectified with center tap return. The system dc output voltages are +5, -14, -5, +24, +14 and +25.

The topmost secondary winding (leads 4, 5 and 6) is the 5 volt winding. After rectification and pi section filtering the +5 volts is provided as feedback to the input regulator M1 and through connection J5D to the base of Q15. Transistors Q14 and Q15 operated as a differential amplifier which results in comparator operation detecting differences between the +5 volts and zener reference voltage (VR 5, +4.7). The results of the comparison provide that the +5 volts must be available first, then the transistors Q16 and Q17 will turn ON, enabling the +14 and +25 volt outputs. The time constant provided by R36 and C8 allows a slight delay after the +5 volts is present before the +14 and +25 volt outputs are enabled. Three voltage levels are fed back to CR7, CR8 and CR9. The bias situation ultimately provides a signal on the base of Q18. Q18 turns off Q19 and produces a system signal called Power Up.

The +14 and +25 volt sections each contain separate dc voltage regulators M3 and M4. In the +14 volt circuitry overcurrent protection is provided by R42, a 0.10 ohm resistor. R44, a 2K potentiometer, allows adjustment of the +14 volts. The components Q24 and R58 have +5 volts applied at point E and function as an emergency load should the normal +14 volt load be disconnected. The +25 volt circuit has overcurrent protection provided by R48 and is voltage adjustable at R50, a 2K ohm potentiometer. The thermistor is physically located on the memory core board and enables the +25 volt to track with temperature variations.

results in comparator operation detecting differences between the +5 volts and zener reference voltage (VR 5, +4.7). The results of the comparison provide that the +5 volts must be available first, then the transistors Q16 and Q17 will turn ON enabling the +14 and +25 volt outputs. The time constant provided by R36 and C8 allows a slight delay after the +5 volts is present before the +14 and +25 volt outputs are enabled. Three voltage levels are fed back to CR7, CR8 and CR9. The bias situation ultimately provides a signal on the base of Q18. Q18 turns off Q19 and produces a system signal called Power Up.

The +14 and +25 volt sections each contain separate DC voltage regulators M3 and M4. In the +14 volt circuitry overcurrent protection is provided by R42, a .10 ohm resistor. R44, a 2K potentiometer, allows adjustment of the +14 volts. The components Q24 and R58 have +5 volts applied at point E and function as an emergency load should the normal +14 volt load be disconnected. The +25 volt circuit has overcurrent protection provided by R48 and is voltage adjustable at R50, a 2K ohm potentiometer. The thermistor is physically located on the memory core board and enables the +25 volts to track with temperature variations.

6.2 KEYBOARD AND CONTROLLER (BOAC)

6.2.1 BOAC Keyboard Model 11-01

The Model 11-01 keyboard maintains the same size physical housing as the standard INCOTERM keyboard. The external appearance is similar except for the operator's surface (see Figure 1). As illustrated, the left and right side mode key areas have been eliminated, as well as the programmed indicator lamps. All required mode keys are located adjacent to the standard alphanumeric arrangement. The keyboard used at the Terminal input is different than the keyboard used at the printer because the need for certain keys is not necessary. Some keys are mechanically locked out (cannot be depressed -- see Operator's Manual for detailed description).

Electronic operation includes operating parameters similar to the standard keyboard, but achieves operation with less components (see Figure 3). The switches are of the reed type and are held in position by a retaining plate. Contact closure results in a specified code output (see Table 1) from the keyboard Read Only Memory (ROM). The ROM is a plugable component and is easily replaced in the field; however, due to the number of pins (40), removal or insertion should be performed with care.

The data strobe line is activated by depressing a key. Interlock logic provides that if any two keys are depressed within 35 ms, and the first depressed is the last to be released, the second key does not generate a character. When activated, the strobe changes from a logical 1 (Quiescent) to a logical 0 (true) where:

logic 1 = -6.5V
logic 0 = +6.5V

When a key is depressed, the strobe is delayed (less than 5 ms) so that the data will be stable when strobed.

Figure 2 illustrates the bottom of the keyboard. Switch replacement or ohmmeter testing can be accomplished from the bottom of the circuit board. Replacement of a switch is accomplished by unsoldering the appropriate leads and removing the switch from the upper retaining plate. Key tops can be

Figure 1. BOAC Model 11-01 Keyboard

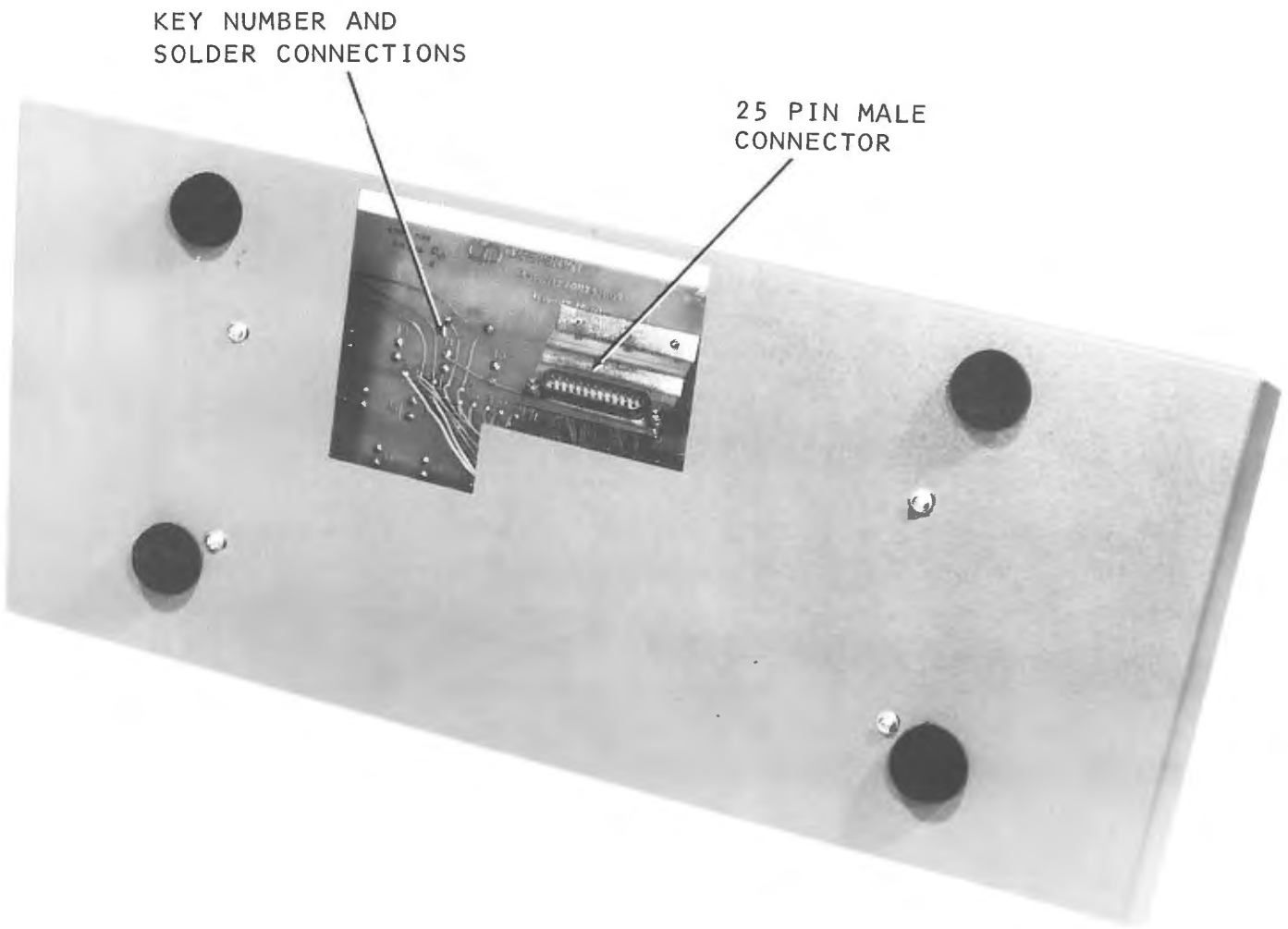


Figure 2 Keyboard, Bottom View

Table 1. Keyboard Coding

KEY #	ALPHA-NUMERIC	BITS 7	6	5	4	3	2	1	KEY #	ALPHA-NUMERIC	BITS 6	7	5	4	3	2	1
1	CLEAR	1	1	0	1	0	0	0	33	S	1	0	1	0	0	1	1
2	1 RLOC	0	1	1	0	0	0	1	34	D	1	0	0	0	1	0	0
3	2 FLFO	0	1	1	0	0	1	0	35	F	1	0	0	0	1	1	0
4	3 GFAX	0	1	1	0	0	1	1	36	G	1	0	0	0	1	1	1
5	4 BFAX	0	1	1	0	1	0	0	37	H	1	0	0	1	0	0	0
6	5 RMKS	0	1	1	0	1	0	1	38	J	1	0	0	1	0	1	0
7	6 RCVD	0	1	1	0	1	1	0	39	K	1	0	0	1	0	1	1
8	7 TKT	0	1	1	0	1	1	1	40	L	1	0	0	1	1	0	0
9	8 TL	0	1	1	1	0	0	0	41	:	0	1	1	1	0	1	0
10	9 PHON	0	1	1	1	0	0	1	42	ENDI	0	1	0	1	1	0	0
11	Ø SEG	0	1	1	0	0	0	0	43	NEW LINE	1	1	0	1	0	1	1
12	NAME	0	1	0	1	1	0	1	44	↑	1	1	0	1	1	1	1
13	RDUC	1	0	1	1	1	1	0	45	DELETE	1	1	0	0	1	1	0
14	$	0	1	0	0	1	0	0	46	CHNG	0	1	0	0	0	1	1
15	DUM	1	1	0	0	0	1	0	47	Z	1	0	1	1	0	1	0
16	FORM FEED	1	1	0	0	1	0	1	48	X	1	0	1	1	0	0	0
17	Q	1	0	1	0	0	0	1	49	C	1	0	0	0	0	1	1
18	W	1	0	1	0	1	1	1	50	V	1	0	1	0	1	1	0
19	EOT	1	0	0	0	1	0	1	51	B	1	0	0	0	0	1	0
20	R	1	0	1	0	0	1	0	52	N	1	0	0	1	1	1	0
21	T	1	0	1	0	1	0	0	53	M	1	0	0	1	1	0	1
22	Y	1	0	1	1	0	0	1	54	. CSS	0	1	0	1	1	1	0
23	U	1	0	1	0	1	0	1	55	* DPLY	0	1	0	1	0	1	0
24	IGN	1	0	0	1	0	0	1	56	+	0	1	0	1	0	1	1
25	O	1	0	0	1	1	1	1	57		1	1	0	0	1	0	0
26	P	1	0	1	0	0	0	0	58	ACTN	1	1	0	0	0	1	1
27	=	0	1	1	1	1	0	1	59	↓	1	1	0	1	1	1	0
28	RESET	1	1	0	1	0	0	1	60	INSERT	1	1	0	0	1	1	1
29	REPEAT	1	1	0	0	0	0	1	61	ENTER	1	1	0	0	0	0	0
30	ERASE CHAR	1	1	0	1	0	1	0	62		0	1	0	0	0	0	0
31	/ IAS	0	1	0	1	1	1	1	63	←	1	1	0	1	1	0	1
32	A	1	0	0	0	0	0	1	64	→	1	1	0	1	1	0	0
									65	,	0	1	0	0	1	1	1
									66	(	0	1	0	1	0	0	0
									67		0	1	0	0	1	0	1
									68	)	0	1	0	1	0	0	1

Key #62 is the SPACE Key

easily removed and no special tools are required to do so.

The keyboard connector wiring is listed in Table 2.

Table 2. Keyboard Connector Wiring

Pin Connector	Function	Pin Connector	Function
1	Ground	17	B7
3	B1	18	+13.5 VDC
5	B2	19	-13.5 VDC
6	B3	20	Keyboard Present
8	B4		
15	B5	22	Strobe
16	B6	25	+5 VDC

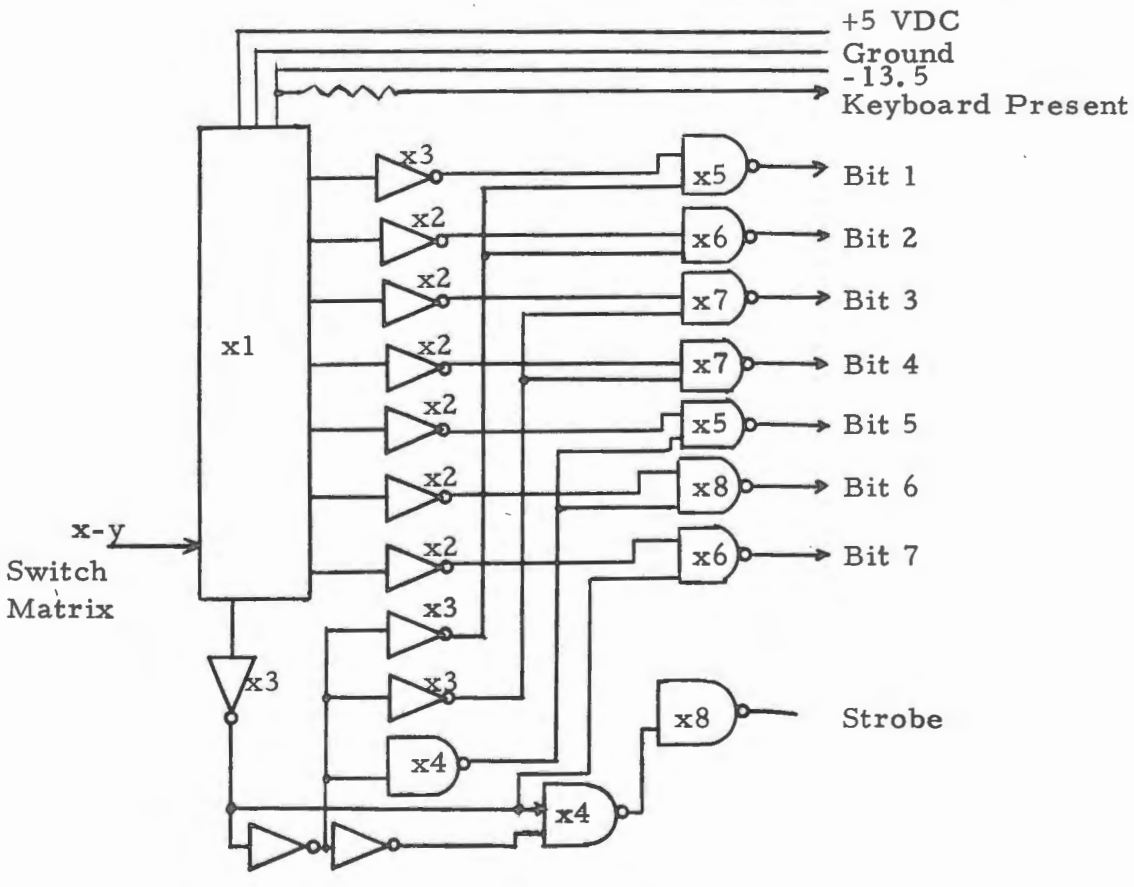


Figure 3. Simplified Block Diagram
Keyboard Electronics With Read Only Memory

6.2.2 BOAC Keyboard Controller

The Keyboard Controller is the keyboard input/TPU interface in the SPD 10/20 system. The controller circuit board is the same size as all other I/O controllers (see Figure 1); however, physical space required for electronic components has been reduced. When compared to the standard keyboard controller, it becomes obvious that much of the space savings is due to the elimination of the eight program controlled lamps. In order that the maximum advantage be taken of the usable area on the circuit board, electronic and printed circuit design have included the possible future use of one controller handling two keyboards. However, initial intended use requires two controllers for a two keyboard operation. The controller electronics also has added circuitry which allows keyboard operation up to 200 feet from the Terminal.

Theory of Operation - The following theory references logic schematic 009-03-01 Rev A (sheet 2) and Figure 2, a simplified block diagram of the BOAC keyboard controller, illustrating the circuitry required in the one keyboard operation. The overall operating conditions can be discussed in conjunction with the keyboard controller timing diagram (Figure 3).

When the KBD STRB goes true (low) the first ready flip flop is set. The next timing phase 2 sets the second ready flip flop which, in conjunction with the TYP, FUNC and INT SEL IN signals, may pass the interrupt (INT SEL OUT) or interrupt for the purpose of transferring data (INTX). A Read I/O addressed to the controller and the Ready condition provides the TPU with an acknowledge and the keyboard data is strobed onto the input bus.

Referring to the schematic, the keyboard strobe is received at input connector pin 58 and line receiver M8. As discussed in paragraph 6.2.1, the strobe is a result of key depression; thus, by definition, if a strobe is present, keyboard data is available. The strobe, when activated, changes from a 1 level to a zero level where: 1 = -6.5V
0 = +6.5V.

The inverted output of M8 is used to clock the first Ready flip flop M11 and is routed to AND gate M22 where it is available for enabling the gate should an

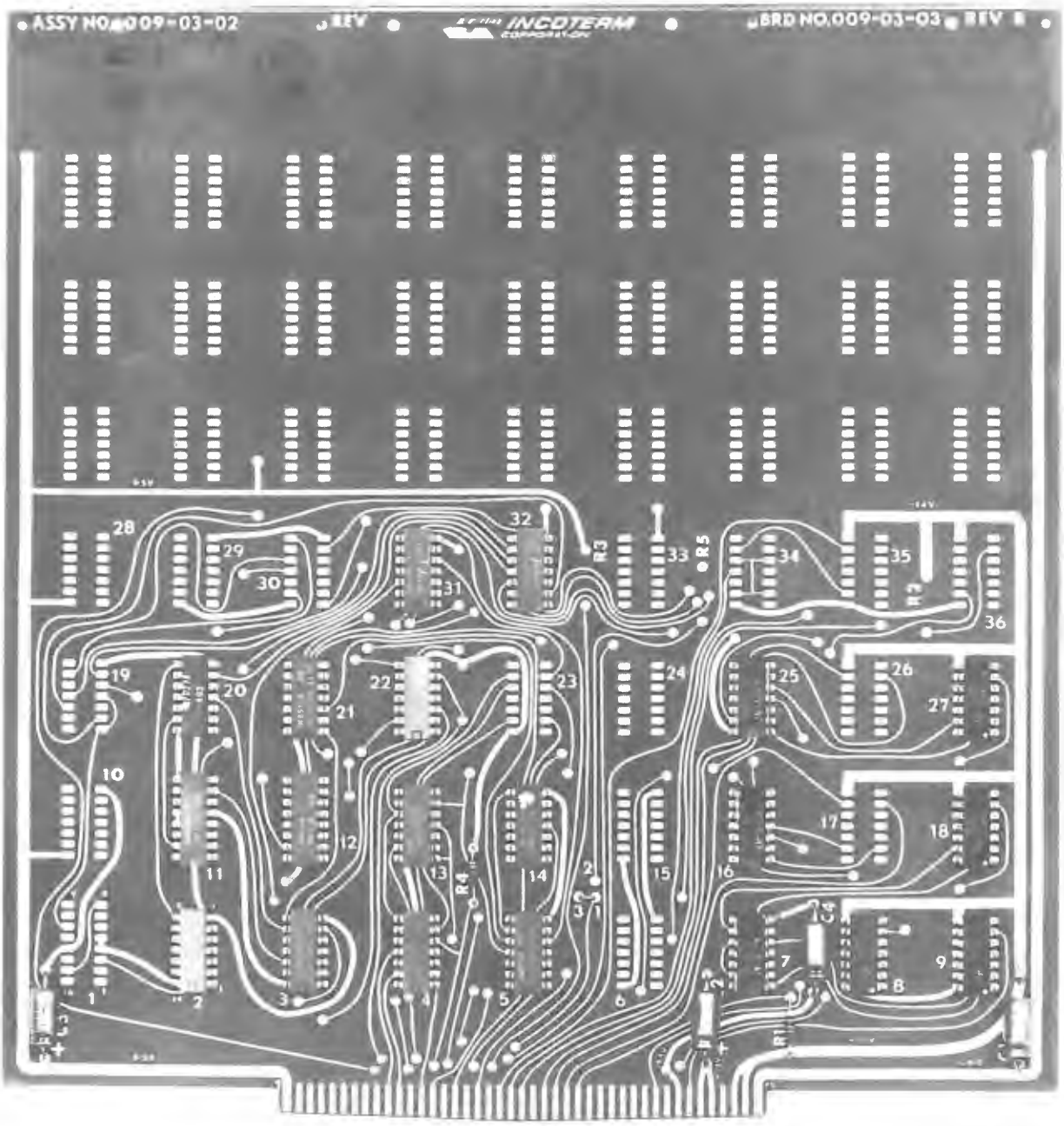


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Figure 1. BOAC Keyboard Controller

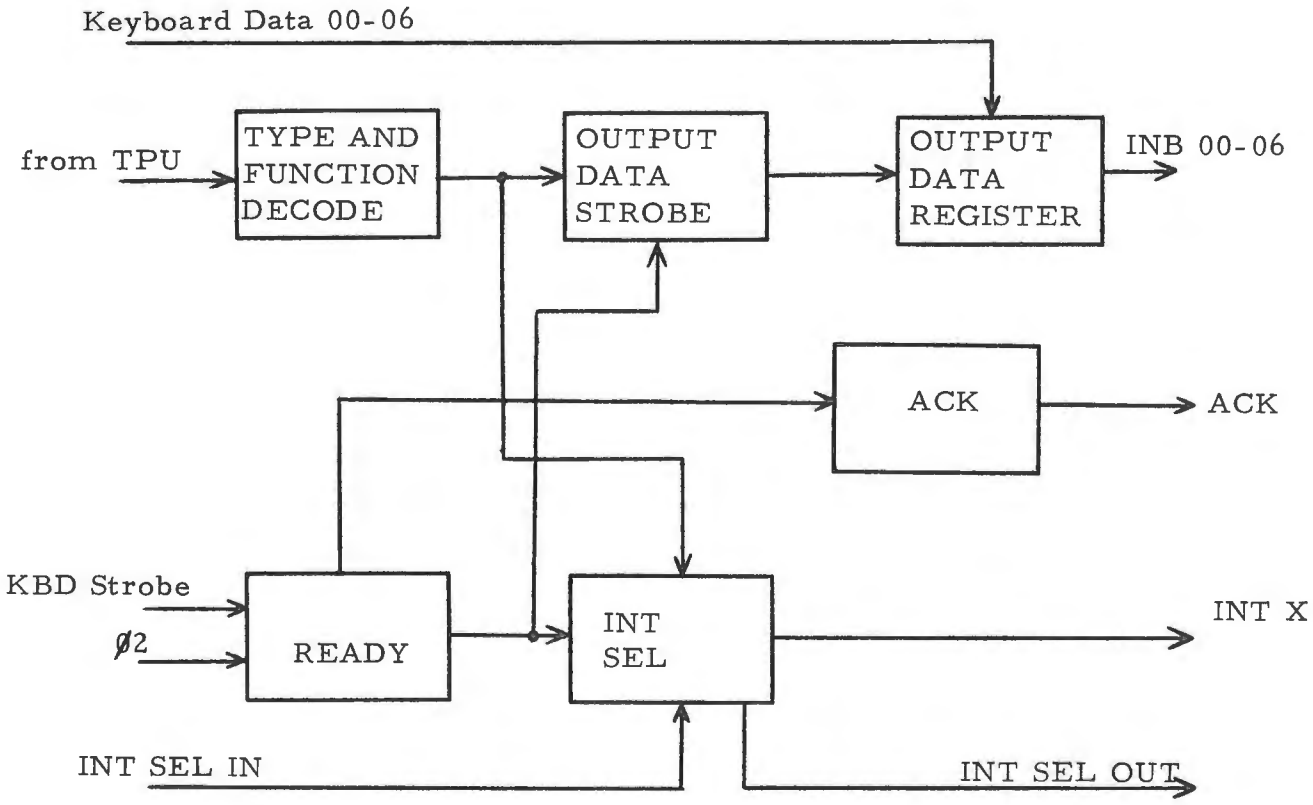

Figure 2. Simplified Block Diagram
BOAC Keyboard Controller

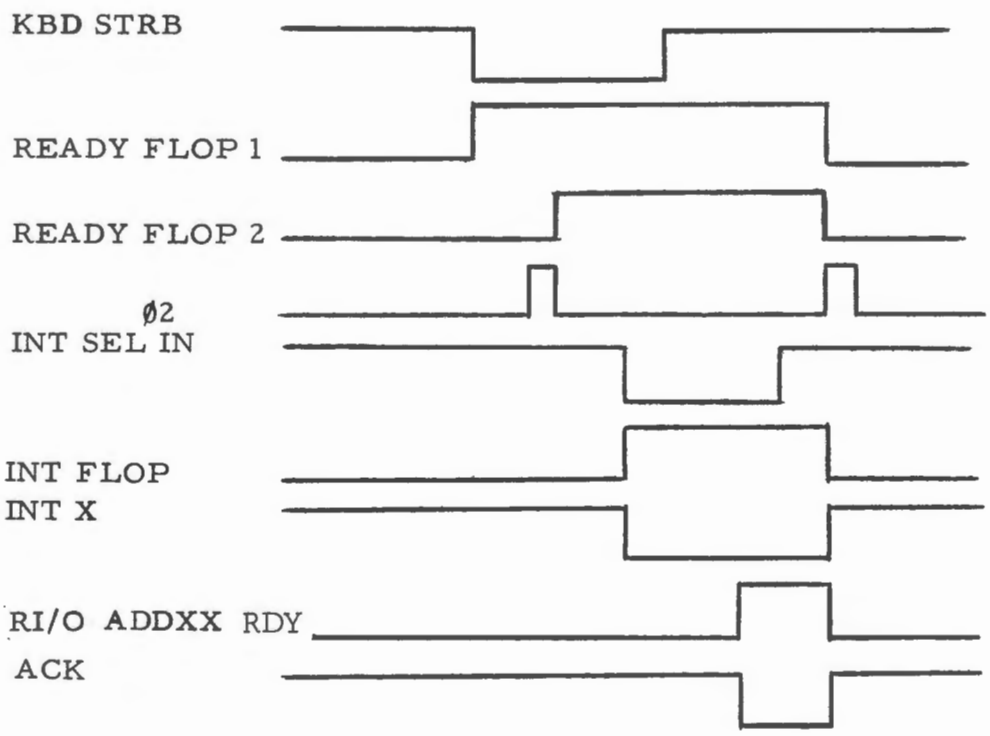

Figure 3. Keyboard Controller Timing

addressed W I/O be issued by the TPU. If the input to M22 is satisfied, the resulting signal logically detects the condition resulting if a key were held down as it would be for a repeat operation. The setting of Ready flip flop 1 (pin 11, Q = 1) conditions the J input of Ready flip flop 2 and on the falling edge of a Ø2 clock the Q output, pin 15, is set (1). The ANDing condition at gate M20 is a function of Ready flop (2) and TPU FUNC code input to flip flop M12 (pins 4 and 16). The function input 02 (hex 4) on input pin 24 is for masking the interrupt and FUNC 03 (hex 8) unmasks the interrupt. When pin 15 of the masking flip flop M12 is Q = 1, the unmask condition is detected at M20 and pin 11 goes true (0). With M20 pin 11 true, the INT SEL IN (Interrupt Select In) signal at input pin 31 is inhibited from passing through M20 to the second keyboard circuit, or passing the select out. The D input of M21 is high and the INT SEL IN signal clocks the flip flop setting Q = 1 and through OR gate M22, the INTX signal is enabled at connector pin 30.

Acknowledge signals are issued to the TPU via pin 27. The ACK gate (M22) can be conditioned by three input signals:

1. a $\overline{\text{R I/O} \cdot \text{ADDXX} \cdot \text{RDY}}$ results in an ACK (M31 pin 6)
2. a W I/O · ADDXX unconditionally acknowledges (M31 pin 1)
3. a Keyboard Present signal ANDed with an addressed T I/O acknowledges (pin 12 M31).

The TPU W I/O addressed to the keyboard controller is part of the repeat key enable function. The W I/O is immediately acknowledged through M31 and M16 and is also ANDed with the keyboard strobe (inverted) signal at gate M22. If a key is held depressed and the programmed W I/O is incorporated, the output signal at M22 is fed to Ready flip flop 1, resulting in a Ready condition which will be true and the data transfer repeats until the key is released.

The strobe signal results from a Read I/O address to the keyboard controller and Ready conditions set. The decoded R I/O is fed to M22 pin 9 where, if Ready flip flop 2 has Q = 0 (not Ready), the signal INTX will be enabled. If Ready 2 has Q = 1, M20 will be true, producing the output strobe and the next T2 will reset Ready 1 in preparation for the next keyboard character.

6.4 ASYNCHRONOUS CONTROLLER (BOAC)

Differences between the standard asynchronous controller and the BOAC async are minimal. The schematic diagram for BOAC is the same number as the standard async (001-04-01 Rev A). The title block contains the designation 002 which is the BOAC designation for this controller.

There is one change on sheet 2. The former clock signal $\overline{DC1}$ was common to logic packages M32, M14 and M5. Due to a noise problem, the clock to M32 is changed to DC1. $\overline{DC1}$ still clocks M5 and M14.

The logic on sheet 3 is changed by addition of new components. The clear input to the T I/O overrun flip flop is ORed with the WRITE mode condition from pin 11 M16. This results in the clear input to M32 being enabled when a system reset occurs or when in the Write mode. At flip flop M53 the clock input is a more stable function of $\overline{BCTODC3}$. The D input in addition to conditioning M53, sets the latch M54 which conditions one input of AND gate M40. When $\overline{BCTODC3}$ is present at pin 2, the clock signal for M53 is generated. The latch is reset by $\overline{1STWRT}$ from M27.

Sheet 4 deals basically with asynchronous timing. Component M9 is utilized to receive the receiver signal timing element. This signal is used with synchronous data sets operating with the asynchronous controller. The signal $\overline{SRC}$ (Serial Receive Clock) is available at option block STB42 pin 5. The internal generated data set clock is also wired to STB42 at pin 7. Either pin 5 or pin 7 can be wired to pin 8, which provides for generation of clock signals as either an internal function of the asynchronous controller or external source.

Sheet 5 contains no changes.

6.5 SYNCHRONOUS CONTROLLER (BOAC)

The Synchronous Controller circuit component locations on the circuit card are modified to include additional components. To meet the additional space requirements, the test block locations and discrete circuit drivers have been replaced by dual in line logic and devices such as Cermetek line drivers and receivers. The schematic logic diagrams reflecting BOAC changes are numbered 001-08-01 Rev A 002, and consist of six sheets, the first one describing only cover sheet information.

The new CM1160 line drivers and line receivers are schematically illustrated on sheet 2. Implementation of the CM1160 allows SPD 10/20 Terminal operation up to 200 feet from the modem.

The received data is fed into the controller on pin 66 where line receiver M62 inverts the data voltage level. The voltage level is provided at option block STB66 pins 2 and 6 in both polarities. The R DATA signal is fed to the serial/parallel shift register M17 on sheet 5. The one shot, M43, provides a 5 millisecond delay after the Request to Send signal has been set. The delayed output signal is fed to option block STB52 pin 14. Component M42 replaces the discrete circuit formerly associated with the NEW SYNC signal. This circuit now provides a program controlled input signal, SET DATA R, which can be optioned at STB66. The transmitted data signal SD OUT can be polarity optioned at STB66.

The circuitry on sheet 3 basically performs the Program decoding and has not been changed a great deal with respect to the standard Sync operation. AND gate M65 has been added to decode the C I/O programmed instructions which result in the SET DATA signal.

Additional components on sheet 4 are M53, M65 and M67. This circuit operates as a decoder of input data. The particular combination of input data required for a true decode is 11 one bits and one zero bit. This signal then synchronizes the controller with the modem.

Sheet 5 contains only one circuit rearrangement. An option block has been inserted in the TPU output bus lines (OTB00-OTB07). This option block can be wired to transpose the TPU data MSB and LSB positions prior to parallel to serial conversion and ultimate transmission.